Master's thesis

Czech
Technical
University
in Prague

F3

Faculty of Electrical Engineering
Department of Microelectronics

Design of an Analog Equalizer for Hall-effect Coreless Current Sensors

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MASTER‘S THESIS ASSIGNMENT

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II. Master’s thesis details

Master’s thesis title in English:

Design of an Analog Equalizer for Hall-effect Coreless Current Sensors

Master’s thesis title in Czech:

Návrh analogového ekvalizéru pro Hallovy bezjádrové proudové senzory

Guidelines:

Familiarize yourself with the current sensing technique using a coreless Hall sensor placed above the busbar's notch and the problems regarding notch frequency behaviour. Simulate frequency responses of the busbar's notch for various parameters of notch and air gap (Width = 2 - 8 mm, Thickness = 2 - 5 mm, Air gap = 1.5 – 3.5 mm). Characterize notch frequency behaviour and find its transfer functions and compensating transfer functions. Propose and compare compensating circuit implementations and choose the most appropriate one.
Design a compensation circuit on the transistor level to compensate for the frequency characteristics of the notch for parameters: Width = 2 - 8 mm, Thickness = 2 - 5 mm, Air gap = 1.5 – 3.5 mm.
Beneficial: If possible, layout the designed circuit.

Bibliography / sources:

E. Ramsden, Hall-Effect Sensors: Theory and Application, 2nd ed. Burlington: Newnes, 2006.
Y. Vuillermet and L. A. Messier, “Methods and Apparatus for Frequency Effect Compensation in Magnetic Field Current Sensors,” Jun. 29, 2021 Available: https://patents.justia.com/patent/20210018573
D. A. Johns and K. Martin, Analog Integrated Circuit Design. John Wiley & Sons, 1997.
P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design. New York: Oxford University Press, 2016.

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Date of master’s thesis assignment: **02.02.2024** Deadline for master's thesis submission: **24.05.2024**

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III. Assignment receipt

The student acknowledges that the master’s thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the master’s thesis, the author must state the names of consultants and include a list of references.

Date of assignment receipt	Student’s signature

Acknowledgements

I would like to thank my supervisors, Prof. Ing. Jiří Jakovenko, Ph.D., and Matthieu Thomas, for their cooperation and guidance throughout my thesis. Also, I would like to express my gratitude to Martin Dřínovský for his valuable advice and sharing his extensive knowledge. Additionally, I would like to thank Stanislav Cvešper for his insights on the layout. And lastly, I would like to express my heartfelt gratitude to my partner, whose unique ability to elevate not only my spirits during the difficult moments working on this thesis has been indispensable.

Declaration

I, Vojtěch Habáň, hereby declare that this thesis titled, "Design of an Analog Equalizer for Hall-effect Coreless Current Sensors," is a record of my original research work. It has been composed by me and all sources used have been cited appropriately.

Prague, 20th May 2024

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Vojtěch Habáň

Abstract

The objective of this thesis is to design an analog equalizer for the coreless Hall-effect current sensor ACS37610, which detects the magnetic field around the notch of a busbar carrying the measured current. Simulations of the notch described its frequency behavior in relation to its dimensions and the sensor's distance, enabling the determination of the compensating transfer function's form. With the transfer function established, a circuit implementation was designed. This thesis utilized a fully differential operational amplifier with switched capacitors as resistors and capacitor matrixes to tune the equalizer, achieving the desired compensating frequency response across a range of notch sizes and sensor distances. The results confirm that the designed equalizer meets the stringent requirements for phase shift and magnitude attenuation across temperature range from -40 °C to 170 °C and voltage ranges from 3-3.6 V and 4.5-5.5 V. The worst-case phase shift after compensation up to 3 kHz is -0.986°, well within the maximum allowable value of 1°. The worst-case magnitude errors after compensation up to 3 kHz are 1.947 % and -5.623 %, both better than the maximum allowable values of 2 % and 10 %, respectively.

Keywords: notch, busbar, frequency response, transfer function, compensation, equalizer, fully differrential operational amplifier, common mode feedback, switched capacitors

Supervisor: prof. Ing. Jiří Jakovenko, Ph.D.

Abstrakt

Cílem této práce je navrhnout analogový ekvalizér pro bezjádrový Hallův proudový senzor ACS37610, který detekuje magnetické pole kolem zářezu vodiče, jímž prochází měřený proud. Simulace zářezu odhalily jeho frekvenční charakteristiky vzávislosti na jeho rozměrech a vzdálenosti senzoru, což umožnilo určení kompenzační přenosové funkce. Po stanovení přenosové funkce byla navržena obvodová realizace. Tato práce využila plně diferenciální operační zesilovač se spínanými kapacitory realizujícími rezistory a matice kondenzátorů pro nastavení frekvenční charakteristiky ekvalizéru kompenzující frekvenční odezvy zářezu pro jeho různé velikosti a vzdálenosti senzoru. Výsledky potvrzují, že navržený ekvalizér splňuje dané požadavky na kopenzaci fázového posunu a amplitudy v teplotním rozsahu od -40 °C do 170 °C a napěťových rozsazích od 3 V do 3.6 V a 4.5 V do 5.5 V. Nejhorší fázová kompenzace do 3 kHz je -0.986°, což je v rámci maximální povolené tolerance 1°. Nejhorší chyby po kompenzaci amplitudy do 3 kHz je 1.947 % a -5.623 % do 20 kHz, oba výsledky splňují požadavky 2 % a 10 % následovně.

Klíčová slova: zářez, přípojnice, frekvenční odezva, přenosová funkce, kompenzace, ekvalizér, plně diferenční operační zesilovač, zpětná vazba společného potenciálu, spínané kapacitory

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List of abbreviations

AC	Alternating Current
AMR	Anisotropic Magnetoresistance
CMFB	Common-mode feedback circuit
CMR	Colossal Magnetoresistance
CMRR	Common-Mode Rejection Ratio
DC	Direct Current
DC-DC	Direct current to direct current converter
EMR	Extraordinary Magnetoresistance
UBW	Unity Gain Bandwidth
GMR	Giant Magnetoresistance
Gm – C	Transconductor with output capacitor
IC	Integrated Circuit
MC	Monte Carlo
MIM	Metal-Insulator-Metal capacitor
MOM	Metal-Oxide-Metal capacitor
MOS	Metal–Oxide–Semiconductor capacitor
PAC	Periodic AC analysis
PCB	Printed Circuit Board
PSRR	Power Supply Rejection Ratio
TMR	Tunnel Magnetoresistance

List of symbols

°	Degrees
dB	Decibels
F	Farads, a unit of capacitance
Hz	Hertz, a unit of frequency
MC1, MC2	Number of connected elementary capacitors in matrixes
N-well	Region in semiconductor fabrication
Ω	Ohms, a unit of resistance
rad/s	Angular frequency
N	Notch's width
T	Notch's thickness
L	Notch's length
AG	Air gap
C	Capacitance of the capacitor
$H(s)$	Transfer function of the circuit
$H(0)$, H_∞	DC gain and gain at infinity, respectively
I_a	Average current
I_b	Biasing current for the operational amplifier
I_{eq}	Current through the equivalent resistor
Q	Charge of the capacitor
R_{eq}	Equivalent resistance
T	Period of the switching clock
V	Voltage
V_{GS}	Gate-source voltage of a transistor
$VNEG$, $VPOS$	Negative and positive supply voltages
V_{id}	Differential input voltage
V_{th}	Threshold voltage of a transistor
V_o^+, V_o^-	Output voltages
f_s	Switching frequency
s	Complex frequency variable in Laplace transforms
μm^2	Square micrometers
ω_p,ω_z	The pole,zero frequency
Φ_1, Φ_2	Non-overlapping clock signals
t	temperature

Chapter 1

Introduction

In recent years, current measurement technology has been becoming increasingly important, and the demand for it is rising. This trend is mainly driven by market growth in the automotive sector, especially electric vehicles, renewable energy, smart grids, and battery management systems. Moreover, alongside market growth, safety requirements for these applications are also increasing, which results in a higher demand for progressively precise current measurement methods. [1] [2]

Among other current sensing methods, Hall-effect current sensors are more and more popular. These sensors enjoy increasing popularity because they combine several key factors. They are suitable for systems that require measurement of both AC and DC currents. Another reason for their popularity is their accuracy, reaching less than 1 %, and a broad bandwidth of measured currents while maintaining a compact form factor, which is particularly beneficial for applications where space is at a premium. [3] [4]

Hall-effect current sensors are also capable of measuring currents ranging from a few amperes to thousands of amperes. This wide variation in measured currents requires different technological implementations of the sensors. For smaller currents, the package integrates the conductor carrying the measured current. While this solution offers high accuracy and compact realization, it is capable of measuring currents only up to 200 A when equipped with special reinforced packages. [3] [5]

For higher currents of up to several thousand amperes, two types of Hall-effect sensors are used: core-based and coreless. Core-based sensors have better performance than coreless ones due to the ferrite core that concentrates the magnetic field onto the sensitive Hall elements of the sensor. However, the core adds significant cost. Coreless sensors represent a low-cost alternative to core-based sensors. [4] [6]

As the coreless Hall-effect sensors are used for the measurement of large currents, they are placed above the notch of the busbar, a large rectangular conductor, to sense the magnetic field generated by the current flowing through the notch. When driving AC currents, through the notch, the varying magnetic field generates eddy currents that disrupt the coupling factor and phase delay of the measured current over frequency. Creating a certain frequency response of the notch. [6] [7] [8] [9]

To enhance the measurement capabilities of coreless Hall-effect sensors, this phenomenon must be compensated for. Since this phenomenon depends on the notch dimensions and the sensor's distance, the required compensation must be adaptable to various attenuations and amplifications across the frequency spectrum. [9] [10]

The main objective of this thesis is to design a compensator for the coreless Hall-effect current sensor ACS37610, developed by Allegro MicroSystems, to address these challenges.

1.1 Objectives of the thesis

The main objective of the thesis is to design a compensator–equalizer for the ACS37610. However, this objective comprises smaller objectives that are necessary to accomplish along the way.

The first objective of this thesis is to simulate the frequency responses of the notch with the following dimensions:

- **Width:** 2-8 mm
- **Thickness:** 2-5 mm
- **Air gap:** 1.5 – 3.5 mm (distance between notch and sensor)

The next objective is to characterize simulated frequency responses and find appropriate transfer functions and compensating transfer functions.

Another objective is to select the most suitable circuit realization for implementation in an integrated circuit.

Finally, design the equalizer with chosen circuit realization able to compensate for all notch frequency responses originating from given dimensions.

The requirements for compensation capabilities of the designed equalizer are the following:

- phase shift less than **1°** up to **3 kHz**
- magnitude attenuation or amplification less than **2 %** up to **3 kHz**
- magnitude attenuation or amplification less than **10 %** up to **20 kHz**

These compensation requirements must be met within a temperature range of -40 °C to 170 °C, as specified by the automotive industry. Furthermore, since the equalizer is designed for the ACS37610, which is manufactured in variants with supply voltages of 3.3 V and 5 V, and the operating voltage range should extend from 3 V to 3.6 V for the 3.3 V device and from 4.5 V to 5.5 V for the 5 V device. The equalizer must also operate within the given requirements at these voltage ranges.

Chapter 2

Current sensing techniques

Electric current measurements are crucial nowadays in many various applications like smart grids and building, clean energy, DC-DC converters and electromobility. With the recent rise in sales of electric vehicles, demand for current measurement also rises. Development and growth of electromobility bring plenty of applications where it is necessary to measure current. Only in the car itself current sensors are used to measure the excitation current within motor's regulation loop, current in each phase of the inverter or current in power disconnect unit to detect overcurrent and quickly disconnect battery. As there are so many applications and most of them are growing it is only appropriate to take interest in this field. [1] [2]

There are various techniques of measuring current. The simplest being shunt resistor, which despite its simplicity poses several disadvantages. Therefore, there is a need for some more advanced methods of current sensing, to mention some of the common ones, magnetoresistors and Hall based sensors.

This chapter is dedicated to the introduction of current sensing techniques. Firstly, various techniques will be introduced shortly and afterwards Hall effect based current sensing will be discussed in deeper detail as this thesis is devoted to the design of an equalizer block for coreless Hall based current sensor.

2.1 Shunt resistor

The simplest method of measuring current is to use a shunt resistor. When measuring current by this method, a shunt resistor is inserted between the load and the source, on which the voltage drop is measured. The current is then calculated by applying Ohm's law. Shunt resistors are special resistors that have a very precise resistance value, which is small, in the order of mOhm. Since the device that measures the voltage across the shunt resistor is connected in parallel to it and has its finite internal resistance, the size of the shunt resistor affects the current measurement error. The main reason for the small values of shunt resistors are the power losses, which are significant even with the low resistance values of the shunt when measuring large currents. As a result, the size and construction of the shunt resistors also increase considerably. Power losses, lack of isolation in high voltage applications

and the size of the construction for measuring large currents are the main disadvantages of measuring current by this method and the reason for the need for other current sensing methods. [11]

2.2 Current transformer

Conventional current transformer is composed of iron core without an airgap and two windings. It is very common that primary winding consists only of one conductor leading trough the core and conducting primary current. In cases where small currents are measured primary winding can be formed by several turns to improve the properties of the current transformer. Secondary winding is wound around the iron core, and it is almost short-circuited. If the core is not saturated, the error of the current transformer is small. For applications with higher requirements on accuracy more advanced core materials are used. [12]

Current transformers are a very accurate technique of current measurement, can be used for measuring high currents and they are galvanically isolated. Their main drawback is that they can be used to measure only AC currents. After magnetization they lose their precision and must be demagnetized. [13]

2.3 Magnetoresistors

Magnetoresistors are sensors based on magnetoresistive effects, which describes dependency of electrical resistance on magnetization of material. Magnetization of material can be changed by applying external magnetic field. Magnetic field can influence the resistivity of material in various ways:

- anisotropic magnetoresistance (AMR)
- giant magnetoresistance (GMR)
- tunnel magnetoresistance (TMR)
- colossal magnetoresistance (CMR)
- extraordinary magnetoresistance (EMR).

as can be observed. [14]

Nowadays, current sensors are often manufactured based on the magnetoresistance principles mentioned earlier. However, each type has its own set of advantages and disadvantages. For example, sensors based on giant magnetoresistance are small and can be used for high frequency applications as they have broad bandwidth, but their linearity is poor. The best choice of magnetoresistor types mentioned above for linear applications are sensors based on anisotropic magnetoresistance. [15]

2.4 Hall effect sensors

To understand how Hall effect sensors work and why they are designed as they are, we will first introduce the Hall effect itself.

2.4.1 Hall effect

The Hall effect was discovered back in 1879 by Edwin Hall, who was inspired by Andre A. Ampere's discovery of a phenomenon that the conductor carrying current experienced a mechanical force when inserted into a magnetic field. Hall wanted to determine whether it was the current or the conductor experiencing the mechanical force. Hall's hypothesis said, that if the force was acting on the current, it would lead to misalignment of the current in the conductor, resulting in a small voltage measurable across the conductor. [16] [17]

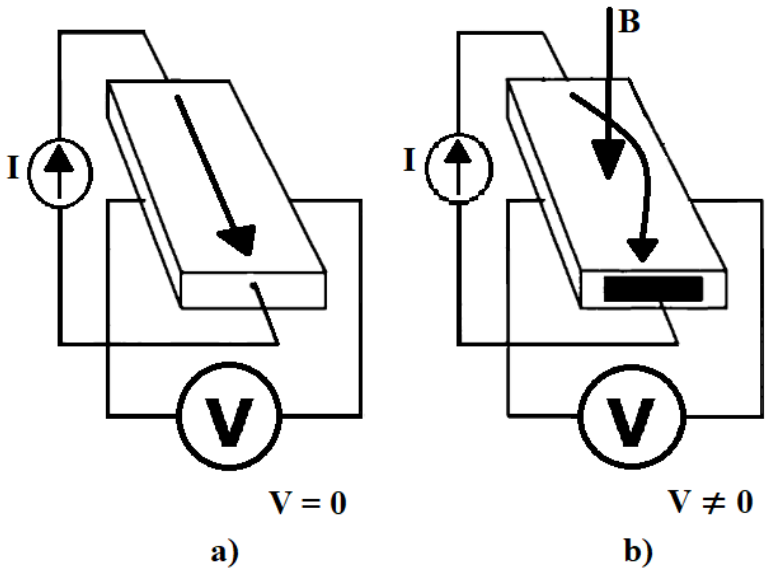

Figure 2.1: Hall effect in conductor

Hall's hypothesis was to a great extent correct. The basic concept of Hall effect can be easily illustrated in Figures 2.1a and 2.1b. In Figure 2.1a there is conductor with two of its sides connected to current source, which sources current I, and voltmeter to perpendicular sides. In this case the conductor is not in magnetic field therefore no voltage is measured between the sides connected to the voltmeter. In Figure 2.1b magnetic field is applied to the conductor in the way that it is at right angle to the current flow. This results in a small voltage measurable on the sides connected to the voltmeter. If the direction of the magnetic field is reversed the polarity of measured voltage is reversed as well. [16] [17]

To deepen the understanding of Hall effect it is important to show the force acting on charged particle moving through electromagnetic field. This force is called Lorenz force, and it is described by Equation 2.1 [16] [17]

$$\vec{F} = q_0\vec{E} + q_0\vec{v} \times \vec{B} \tag{2.1}$$

where

$\vec{F}$	is the resultant force,
q_0	magnitude of the charge,
$\vec{E}$	electric field,
$\vec{v}$	velocity of the charge and
$\vec{B}$	is the magnetic field.

From the Equation 2.1 we can observe that electric field pulls charged particle in the direction of the field, however magnetic field does not have any effect on the particle unless it is moving. If the particle is moving the resulting force is a function of direction of its velocity, orientation of magnetic field it is moving through and its charge. Consider the situation in Figure 2.2, where $\vec{v}$ and $\vec{B}$ are at right angles, therefore $\vec{F}$ is at right angles to both. In this situation velocity and electric field are constrained only to z axis and magnetic field only to y axis, therefore Equation 2.1 can be simplified to Equation 2.2. [16] [17]

$$F_x = -q_0 v_z B_y \tag{2.2}$$

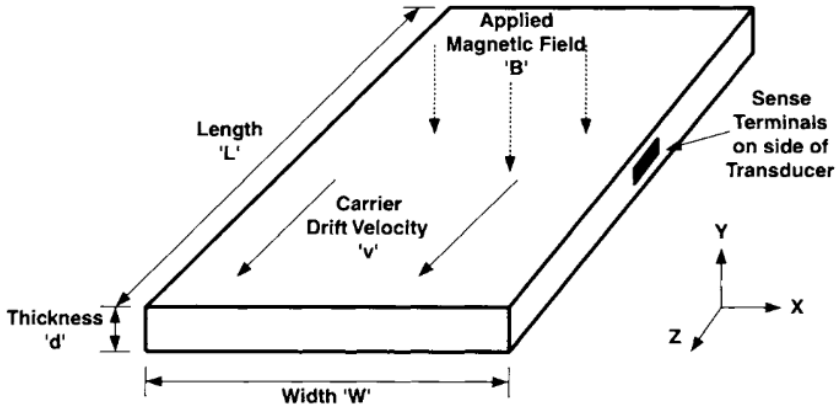

Figure 2.2: Hall effect transducer with necessary dimensions and axis [O1]

As magnetic field forces particles to the one side of the Hall transducer it creates depleted region on the other side. This forms an electric field across the x axis of the transducer, which opposes the force caused by magnetic field and tries to redistribute particles more evenly. When these forces are balanced out equilibrium is developed, which can be described by Equation 2.3. [16] [17]

$$q_0 E_H + q_0 v_z B_y = 0 \tag{2.3}$$

Where E_H is Hall electric field across the transducer. Solving for E_H gives Equation 2.4.

$$E_H = -v_z B_y \tag{2.4}$$

Hall electric field E_H can be integrated, assuming it is uniform, over w to give Hall voltage V_H between sense terminals on the transducer as shown in Eqation 2.5.

$$V_H = -w v_z B_y \tag{2.5}$$

As Figure 2.2 and equations above imply Hall effect sensors have "sensitive" axis which is perpendicular to direction of current flow and sense terminals, also the Hall voltage is linear function of charge carrier velocity, magnetic field applied in the "sensitive" axis and the distance between sense terminals. [16] [17]

When Hall effect was discovered, it was observed using metals, even though Hall-effect voltage in metals is extremely small and hard to measure. Nowadays semiconductors are used because they have various advantages over metals. In semiconductors Hall effect is easier to measure because they have less carriers per unit of volume, also they can be doped to desired concentration of dominant charge carrier. Another advantage is that Hall transducers can be easily integrated into modern integrated circuits. [16] [17]

2.4.2 Types of Hall effect sensors

Hall effect sensors are currently employed across a wide range of uses. They are utilized in DC/DC converters to detect small currents of a few amperes at rapid switching rates, as well as in high voltage traction motor inverters to measure currents in the thousands of amperes. The substantial variation in the magnitude of currents being measured necessitates distinct approaches to the packaging and application of current sensors. [3] [5]

Hall based sensors implementation can be divided into two main categories depending on the position of conductor carrying measured current. Both implementations with its types and benefits of each type are shown in Figure 2.3. [3] [5]

The first possible implementation has a current carrying conductor integrated within IC's package. As can be seen in Figure 2.3 this implementation can be further divided into two types, for low voltage applications and packages with basic and reinforced isolation. The integrated conductor forms a meander around hall plate transducer implemented in the IC. The limitation of this implementation is self-heating caused by measured current flowing through the package of the sensor. Due to heating limitation of this implementation, it is usable only for lower currents up to few hundreds of amperes, however sensing bandwidth of these parts is much better in comparison to those with external conductor, reaching 1 MHz. [3] [5]

Implementation with external conductor can be divided into types as well. The first type being core based sensors which are placed into the airgap

in ferromagnetic core embracing conductor with measured current. These sensors have excellent performance. However, the necessity of ferromagnetic core makes them expensive and big to implement. On the other hand, their counterparts, coreless sensors, are low cost and small solutions. [4] [6]

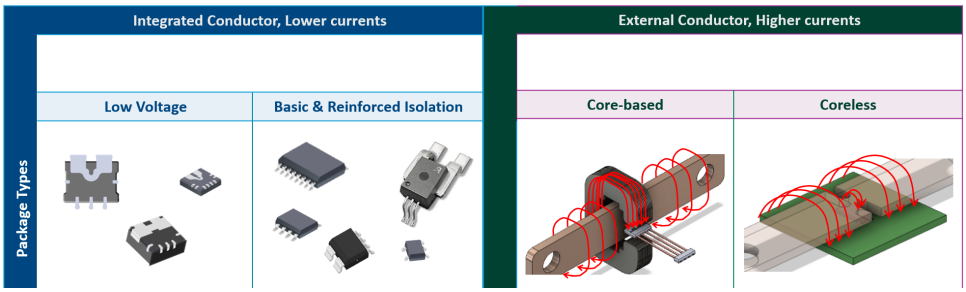

Figure 2.3: Overview of Hall based sensor types

Chapter 3

Coreless current sensing and its drawbacks

As mentioned in Section 1.4.2, coreless sensors offer a cost-effective solution for determining the magnitude of hundreds or thousands of amperes. The low cost of this solution is thanks to the absence of a concentrator core or a U-Shaped Magnetic Shield. [6]

High accuracy is attained by using two Hall elements, which measure the difference in the magnetic field generated by the current flowing in the conductor, as illustrated in Figure 3.1a. The differential configuration of Hall elements provides excellent immunity to stray magnetic fields without the need for a magnetic shield, which slows down the response time and adds nonlinearity-error. [6]

Configuration of coreless current measurement setup is outlined in Figure 3.1b. A current sensor is placed on the PCB close to the conductor carrying measured current, which is called busbar. The location of the sensor is situated above a notch, although it is not utilized in all busbars. Nonetheless, it enhances the current density and further enhances the signal-to-noise ratio of the system. [6]

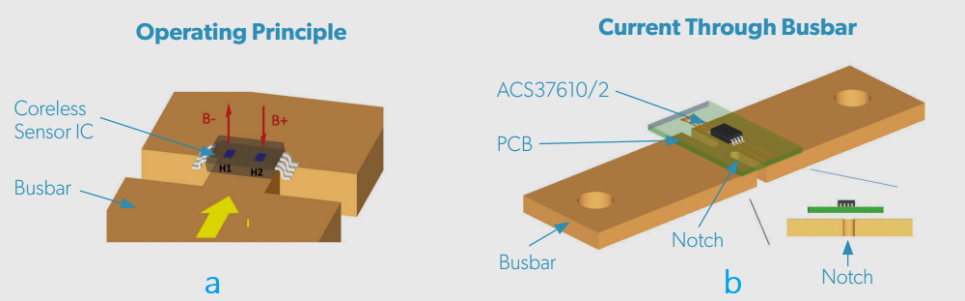

Figure 3.1: Operating principle and measurement configuration of coreless current sensor [O2]

To achieve measurement with the highest resolution, it is necessary to have the highest coupling factor. The coupling factor between the notch and sensor depends on the design parameters of the notch and sensor placement, especially on the notch's width (N), thickness (T) and air gap (AG) between the sensor and notch. The mentioned dimensions are illustrated in Figure 3.2. The air gap and thickness cannot be changed easily, that leaves width as

the main parameter. Driving an AC current through the busbar generates variable magnetic field, which leads to changes in coupling factor, that is characterized over frequency. [8] [10]

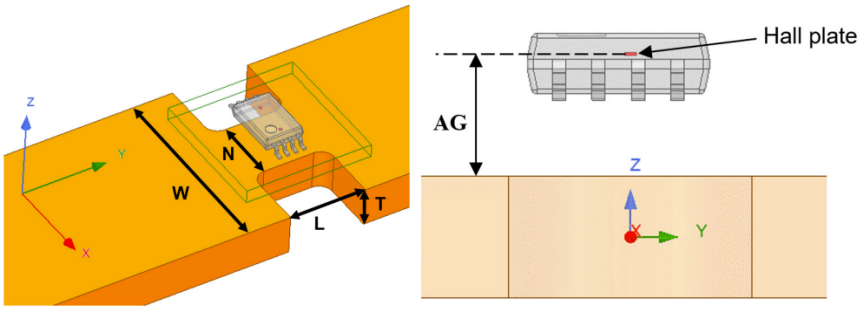

Figure 3.2: Notch and sensor placement dimensions [O3]

3.1 Frequency behavior of the busbar

As mentioned previously, a sensor is placed near the conductor carrying the measured current, to sense the magnetic field generated by the current. The output generated by the sensor is proportional to the magnetic field generated by the current and therefore to the current itself. However, when driving AC currents, the accuracy with which the current is sensed by the sensor is affected, because the varying current generates a varying magnetic field, which tends to generate eddy currents. [8] [10]

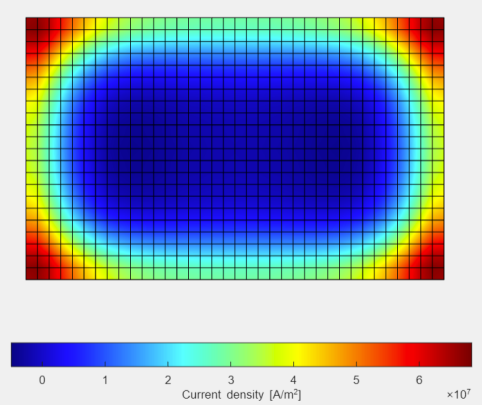

Figure 3.3: Notch current distribution ($N = 8$ mm, $T = 5$ mm, $f = 10$ kHz) [O4]

If the conductive body, the busbar, is carrying a time-varying current, it is therefore subjected to a time-varying magnetic field. Consequently, voltages are induced in this body, which cause circulating currents within the body. These currents are called eddy currents. Their presence in the conductor results in a non-uniform distribution of current density in the cross section of the conductor. The current density becomes higher near the surface at higher

frequencies. Variations of the current density also lead to modifications in the magnetic field distribution around the conductor, the notch. In Figure 3.3, the current density is visualized for the notch with dimensions $N = 8$ mm and $T = 5$ mm and current of 650 A with 10 kHz frequency. [7] [8] [9] [10]

Due to changes in distribution of magnetic field around notch, differential magnetic field measured by the sensor is different compared to DC current measurement. This relates to changes in coupling factor and phase delay in the measured current over frequency. [9] [10]

This phenomenon of eddy currents in the busbar and its notch is the main drawback of current measurement with coreless Hall based sensors and it is the limitation for bandwidth of the current measurement. [9] [10]

To compensate for the effect of eddy currents and consequent variations in coupling factor a compensation factor with inverse characteristic should be applied to flatten the frequency response of the original coupling factor. [9]

3.2 Notch frequency characteristics in dependency on its dimensions

Notch dimensions have significant influence on coupling factor variations over frequency. This chapter is dedicated to illustrate the relations between variations in notch width (N), thickness (T) and airgap (AG) and the resulting coupling factor variations. Notch dimensions that are considered for simulations are in Table 3.1, as those are values used in most applications. [8] [10]

	Minimal (mm)	Typical (mm)	Maximal (mm)
N	2	3-6	8
T	2	3-4	5
AG	1.5	2.5	3.5

Table 3.1: Used notch dimensions

These simulations are performed for the setup shown in Figure 3.2. They are run in a simulator created by Allegro MicroSystems, that is, “Busbar Notch Field Simulation for AC and DC Coreless Current Sensor”. [18] The simulations are 2D and assume infinite length (L) of the notch. This assumption is valid for $L > 10$ mm, because under this condition the eddy currents in a large body of busbar do not affect the measurement. [10] [18]

As can be seen in Figure 3.4 notch frequency characteristic slightly attenuates higher frequencies. Maximal coupling factor variation in this case is approximately -1.1 % and phase shift is less than -0.4°.

However, in Figure 3.5, where the notch has width and thicknes twice of those in Figure 3.4, the attenuation and phase shift are much more significant. Maximal coupling factor variation is more than -10 % and phase shift -3°. Moreover, noticeable attenuation begins on lower frequencies for larger dimensons of the notch.

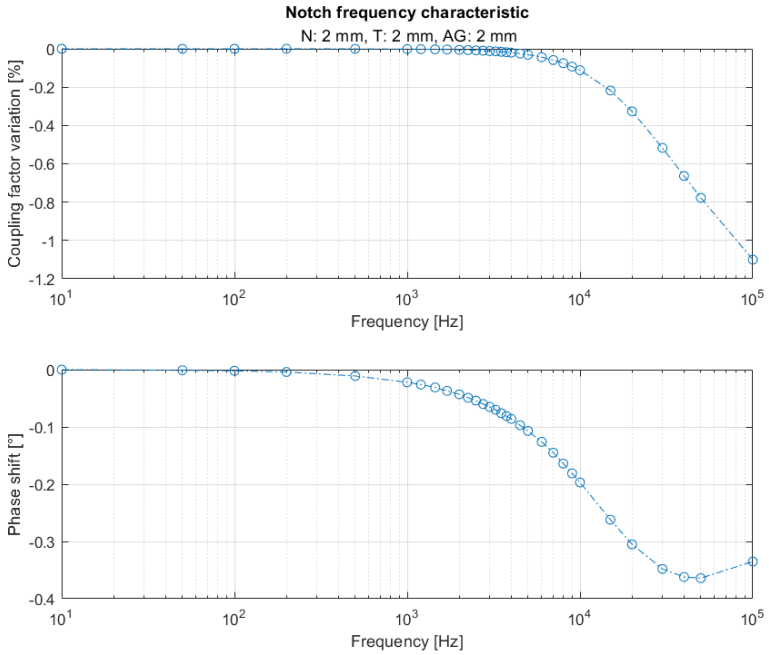

Figure 3.4: Notch frequency characteristic ($N = 2$ mm, $T = 2$ mm, $AG = 2$ mm)

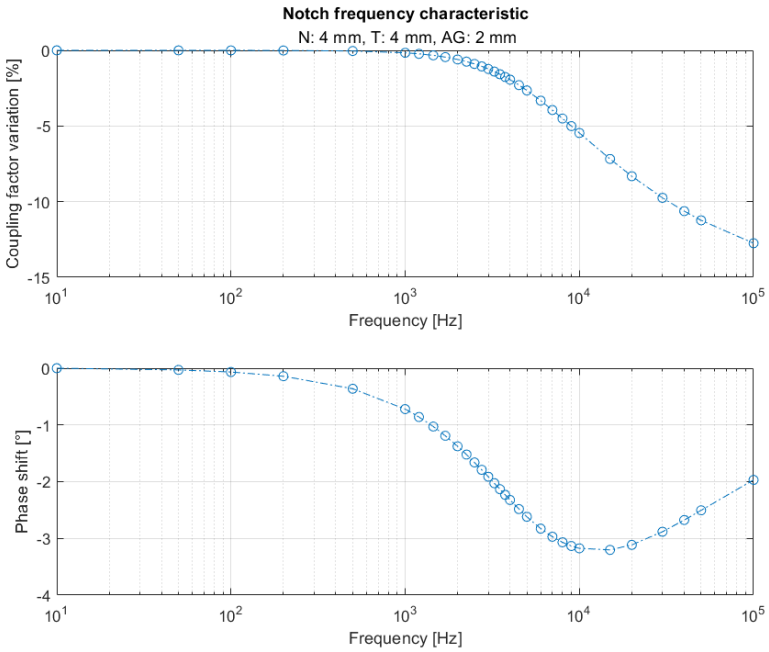

Figure 3.5: Notch frequency characteristic ($N = 4$ mm, $T = 4$ mm, $AG = 2$ mm)

In Figure 3.6 frequency characteristic for maximal notch dimensions is shown. Attenuation and phase shift are much more significant than in previous cases reaching more than -50 % coupling factor variation and more than -15° phase shift.

Situation when thickness is greater than width is illustrated in Figure 3.7.

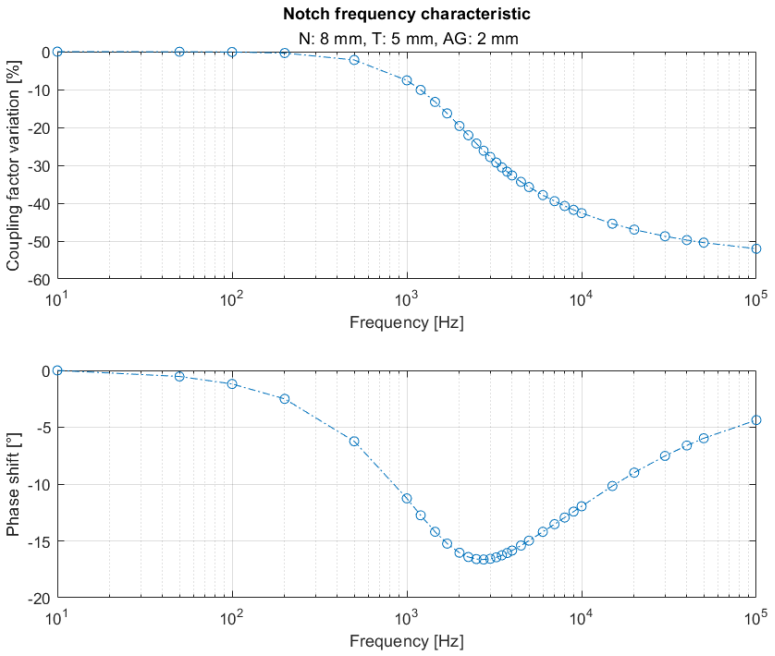

Figure 3.6: Notch frequency characteristic ($N = 8$ mm, $T = 5$ mm, $AG = 2$ mm)

This frequency characteristic has opposite result to the previous ones and amplifies on high frequencies, whereas phase shift is positive.

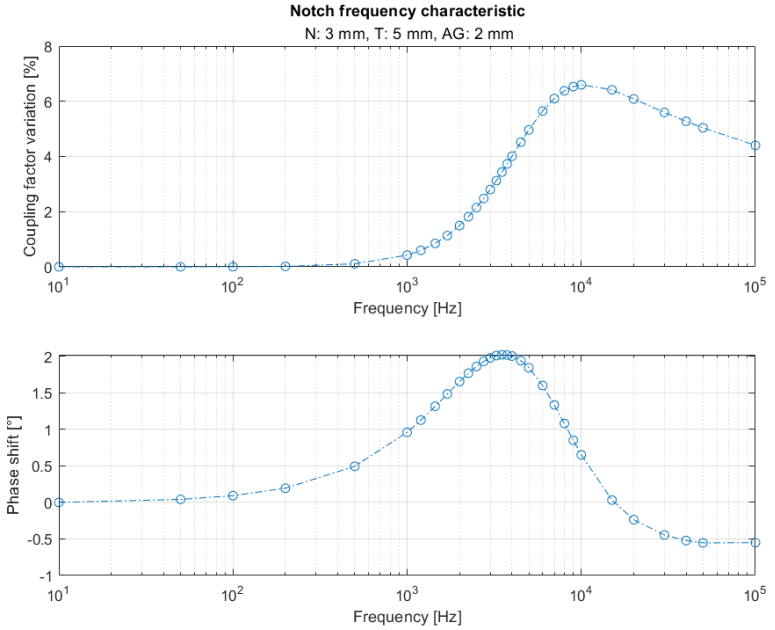

Figure 3.7: Notch frequency characteristic ($N = 3$ mm, $T = 5$ mm, $AG = 2$ mm)

At last Figure 3.8 illustrates influence of air gap on the frequency characteristic of notch. Simulation is run for the maximal dimensions of the notch and air gap values mentioned in Table 3.1. As can be seen in Figure 3.8 smaller

air gap results in greater attenuation and phase shift.

In conclusion, greater dimensions resulted in greater coupling factor variations and phase shifts (frequency response of the notch). For cases when the notch's width is larger or equal to its thickness (Figures 3.4, 3.6), the coupling factor was attenuated and for the opposite amplified (Figure 3.7). This can be reasoned with the current distribution in Figure 3.3, because on higher frequencies the current density is highest in the corners of the notch and therefore it is higher on the shorter side of the notch. Because the variation of the coupling factor and the phase shift is greater with greater dimensions and with a smaller air gap, the attenuation and phase shift for the case when $N = 8$ mm, $T = 5$ mm, and $AG = 1.5$ mm is very significant. The maximal values of deviation from DC value are -61.96 % for the coupling factor variation and -22.15° for the phase shift.

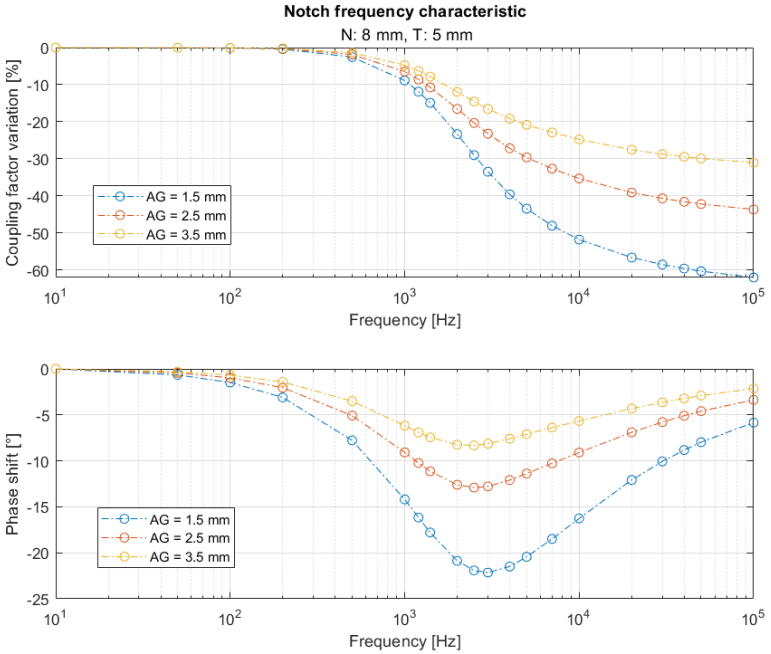

Figure 3.8: Notch frequency characteristics for various air gaps ($N = 5$ mm, $T = 8$ mm)

The simulator provides data of the notch frequency characteristics. The variability of these characteristics is the main drawback of coreless current sensing, this demands the implementation of compensation of this phenomenon and improve this measurement method. [18]

Chapter 4

Notch frequency response characterization and compensation

As stated in Section 1.1, the objective of this thesis is to design a compensator for coreless current measurement to compensate for coupling factor variations caused by eddy currents in the notch. This compensator should be able to compensate for frequency characteristics of the notch from minimal to maximal used dimensions and the air gap between the notch and sensor. These dimensions are listed in Table 3.1. The requirements for the signal after compensation are the following:

- phase shift less than 1° up to 3 kHz
- magintude attenuation or amplification less than 2 % up to 3 kHz
- magnitude attenuation or amplification less than 10 % up to 20 kHz

4.1 Approximating transfer functions

The first step to designing a compensator is to find the correct transfer functions of notch frequency behavior. An analysis of Figures 3.4–3.8 reveals that the notch's frequency behavior can be approximated with a standard filter. For cases when the width is greater than the thickness notch frequency characteristic is a low pass filter, however for cases when the notch's thickness is greater than its width it behaves as a high pass filter or band pass filter.

Taking Figure 3.6 as an example for characterization, attenuation on higher frequencies and negative phase shift indicates pole, nevertheless on higher frequencies phase shift has growth towards its initial value and trough is formed on phase shift characteristic. That suggests that the transfer function also possesses a zero on higher frequencies, which is also supported by the flattening of the curve of magnitude frequency characteristic (coupling factor). These observations suggest that notch's frequency characteristics can be described by first-order transfer function with one pole and one zero.

To clarify, if previous assumptions about transfer function were correct, Matlab and its functions for estimation of transfer functions were used. Because the simulator gives only discrete values in a few points the output

data had to be interpolated. The data interpolation was done using a Matlab function called *pchip* which implements piecewise cubic interpolation. The curves resulting from the interpolation are used to estimate the transfer function using the *tfest* function. These estimates confirmed the previous assumption because the best-fitting estimate was the first-order transfer function with one pole and one zero. After finding the correct form of transfer function it was necessary to determine the accurate position of the pole and zero for all possible dimensions of notch spanning from 2x2 mm to 8x5 mm and for air gaps from 1.5 mm to 3.5 mm. All dimensions were incremented with a 0.1 mm step. This was done using the *fminsearch* function.

Because of the requirements which state much more accurate compensation on frequencies up to 3 kHz also criteria of selection of the best approximating transfer functions was done with greater emphasis on minimizing errors on frequencies up to 3 kHz.

In Figure 4.1 is an example of notch frequency characteristics and its best approximating transfer function which is written in Equation 4.1.

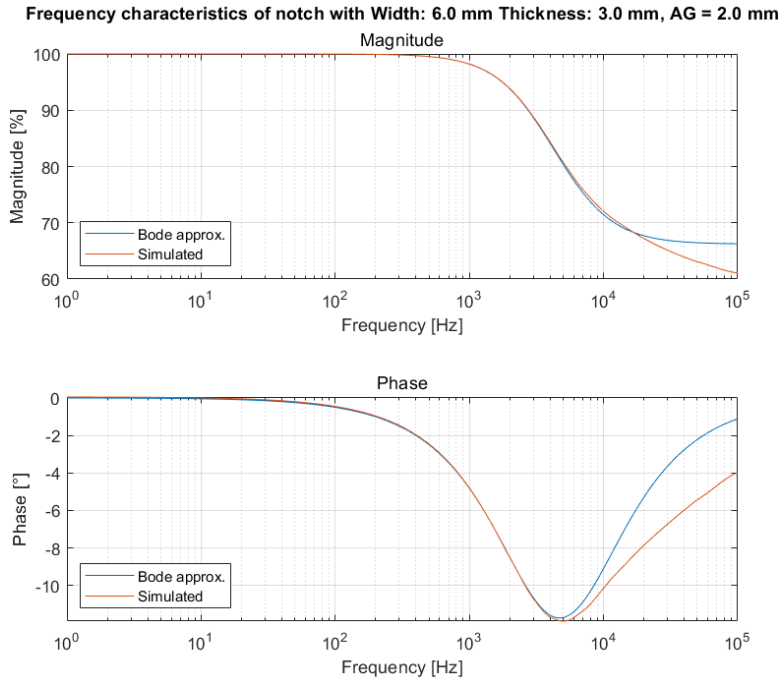

Figure 4.1: Notch frequency characteristics and its best approximating transfer function (N = 6 mm, T = 3 mm, AG = 2 mm)

$$H(s) = \frac{0.6621s + 24089}{s + 24089} \tag{4.1}$$

The values of pole and zero are s_p = -24 089 rad/s and s_z = -36 385 rad/s. Maximal deviation of approximation from simulation result up to 3 kHz is 0.13 % for magnitude and 0.051° for phase shift. The error of Bode approximation from simulated frequency characteristic is visualised in Figure 4.2.

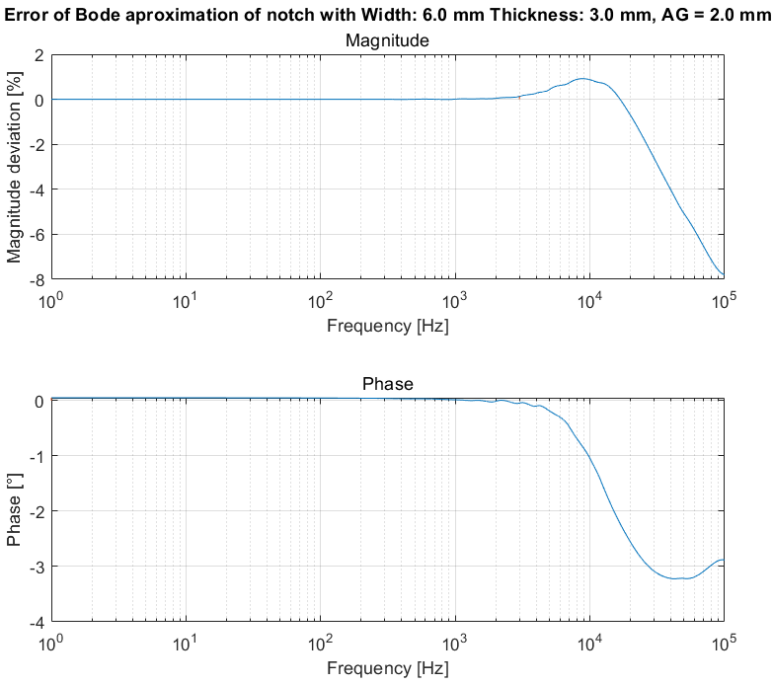

Figure 4.2: Error of approximating transfer function from simulation ($N = 6$ mm, $T = 3$ mm, $AG = 2$ mm)

Both pole and zero are in the left half-plane on the real axis. The position of zero and pole for various dimensions of busbar can tell a lot about their influence on frequency characteristics. This is illustrated in Figure 4.3.

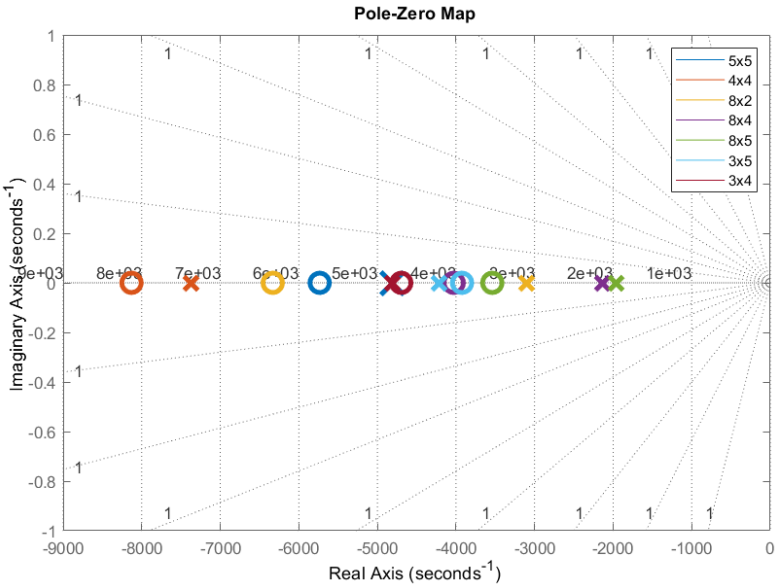

Figure 4.3: Pole and zero possitions of approximating transfer function in relation to notch dimensions

Figure 4.3 illustrates positions of poles and zeros for several notch dimensions. From plot for notch 4x4 mm and 5x5 mm is apparent that greater dimensions place poles and zeros on to lower frequencies which means lower cutoff frequency of frequency characteristic. From plots for notch dimensions 8x2 mm, 8x4 mm, 8x5 mm is clear that with bigger difference between width and thickness pole and zero move away from each other, which results in higher attenuations and phase shifts. Therefore, notch with 8x5 mm dimensions has lowest cutoff frequency and with dimensions 8x2 mm has highest attenuation and phase shift. For cases when width is smaller than thickness positions of zero and pole are opposite to previous cases and zero is located on lower frequency than pole.

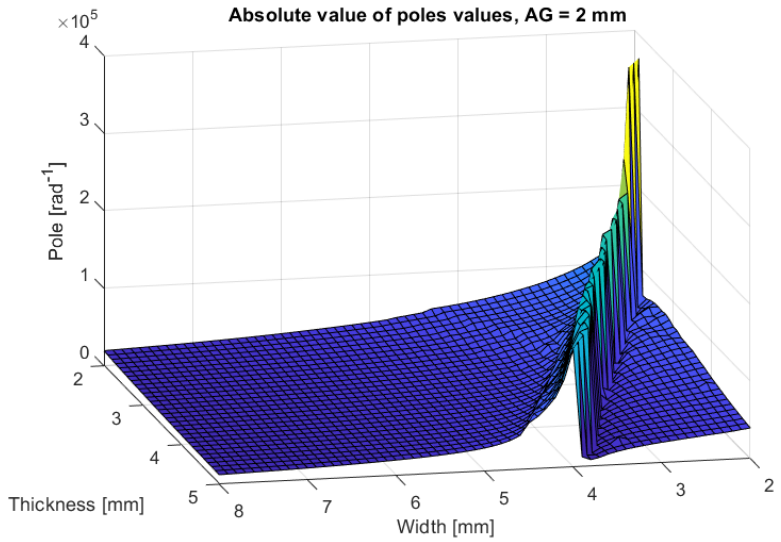

Figure 4.4: Absolute values of poles for all notch sizes ($AG = 2$ mm)

Characterization of locations of poles and zeros for all combinations of notch dimensions and air gap $AG = 2$ mm is illustrated in Figure 4.4 and Figure 4.5, for better lucidity absolute values are plotted. Results are not as continuous as expected and "cliff" is formed in the middle of the plot. This "cliff" is caused by problematic approximations for notch dimensions when width is slightly smaller than thickness. In Figure 3.7, from previous chapter there is visible slight attenuation on frequencies above 10 kHz after rise in in gain between 1 kHz and 10 kHz. For the cases placed on the "cliff" the part of the frequency characteristics where signals are amplified becomes negligible and the attenuation on higher frequencies is much more significant as illustrated in Figure 4.6. Therefore the chosen approximating transfer functions have low pass characteristics, however due to gain peak their cutoff frequency is much higher than in other cases.

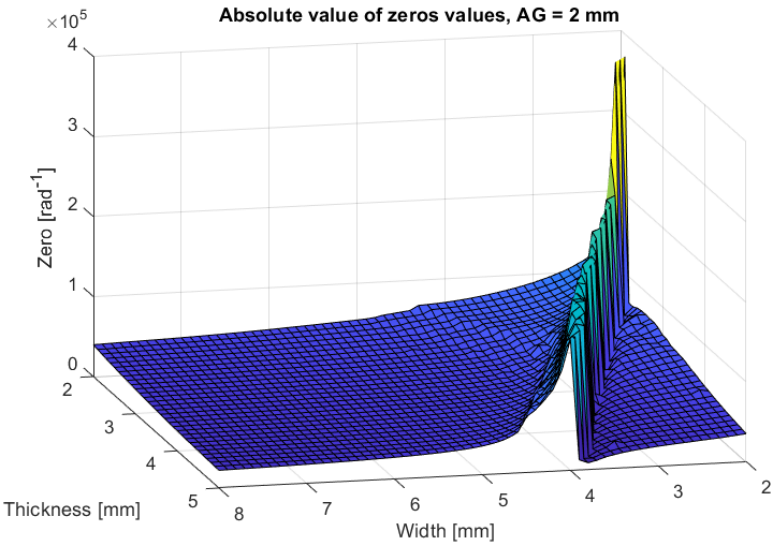

Figure 4.5: Absolute values of zeros for all notch sizes ($AG = 2$ mm)

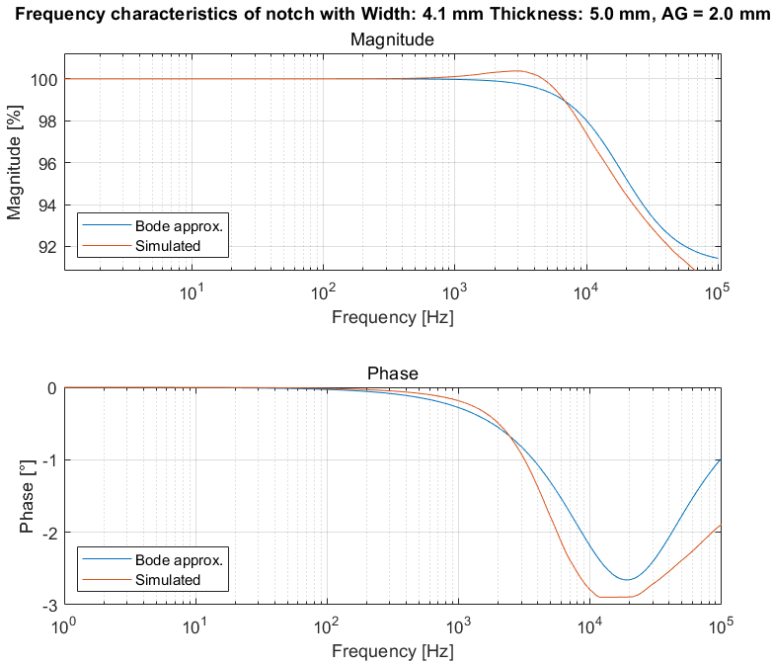

Figure 4.6: Notch frequency characteristic forming peak in gain ($N = 4.1$ mm, $T = 5$ mm, $AG = 2$ mm)

4.2 Compensating transfer functions

In an ideal scenario, the application of compensation would result in frequency response represented by horizontal line. Nonetheless, discrepancies have arisen during the process of approximating the simulated results. Finding compensating transfer function is basically finding system function of certain

system, which is defined as Laplace transform of the output signal divided by Laplace transform of input signal. This relation is depicted in Equation 4.2, where *H(s)* is desired compensating system function, *X(s)* represents transfer function approximating notch frequency behavior and *Y(s)* represents the result after ideal compensation. [19]

$$H(s) = \frac{Y(s)}{X(s)} \tag{4.2}$$

To obtain compensating transfer function *X(s)* and *Y(s)* are to be substituted by their formulas. *Y(s) = 1* over all frequencies and the *X(s)* representing transfer functions approximating notch frequency behavior is Equation 4.3. [19]

$$X(s) = H_{N\infty}\frac{s+\omega_z}{s+\omega_p} \tag{4.3}$$

Where

$H_{N\infty}$	is gain in infinity,
ω_z	is cutoff frequency formed by zero and
ω_p	is cutoff frequency formed by pole.

Relation between zero s_z and ω_z is $\omega_z = -s_z$, respectively for pole s_p and ω_p is $\omega_p = -s_p$. If *X(s)* and *Y(s)* are pluged in to the Equation 4.2 it becomes Equation 4.4, which can be simplified to form in Equation 4.5. [19]

$$H(s) = \frac{1}{H_{N\infty}\frac{s+\omega_z}{s+\omega_p}} \tag{4.4}$$

$$H(s) = \frac{s+\omega_p}{H_{N\infty}(s+\omega_z)} \tag{4.5}$$

From Equation 4.5 it is apparent that compensating transfer function has same form as the approximating transfer function, but values of pole and zero are switched and gain in infinity is its own inverse. Therefore these two transfer functions can be easily converted to each other. [19]

Chapter 5

Selection of compensating circuit implementation

A possible circuit implementation for compensating the frequency behavior of the notch is an analog active filter. Since the notch has first order frequency characteristics the architecture of the filter will be quite simple. There are several possible ways to implement the active filter and each of them has its benefits and drawbacks. The significant dependency of notch frequency characteristic on its dimensions requires compensation filter to be tunable. The considered implementations are following:

- **Active RC filter**, illustrated in Figure 5.1, is the first possible circuit implementation of compensating transfer functions. This circuit is an operational amplifier in inverting configuration. The values of resistors and capacitors determine pole and zero positions therefore, to realize various transfer functions they must be adjustable. To achieve various transfer functions capacitors C_1 and C_2 can be composed from matrixes of small capacitors which are connected as needed. As the capacitors and resistors are not ideal for integration this solution can result in a huge silicon area.

- **Switched capacitors filter** is illustrated in Figure 5.2. The resistors in circuit in Figure 5.1 are replaced by delay-free switched capacitors. With this replacement resulting switched capacitors filter has the same low-frequency behavior as its active RC in Figure 5.1. Using switched capacitors huge values of equivalent resistors can be realized on small area moreover switched capacitors are suitable for integration and can be easily tunable, by changing their switching frequency. However, the necessity to tune both pole and zero of the filter transfer function, two different clock signals are required. Changing switching frequency and therefore equivalent resistors also changes the DC gain of the filter which is not suitable for this application.

- **gm − C filter** is also considered implementation; however, it is the least suitable one as it has the same drawback as switched capacitors of changing DC gain while tuning the filter. Moreover gm–c filters face problems with linearity.

- Last considered implementation is combination of active RC and switched capacitors filters. This implementation can also be realized by the circuit in Figure 5.2. Resistors are replaced using switched capacitors to reduce silicone area used, but they have common clock source, which is invariable. The tuning of the filter is realized by C_1 and C_2 which are composed of matrixes of small capacitors.

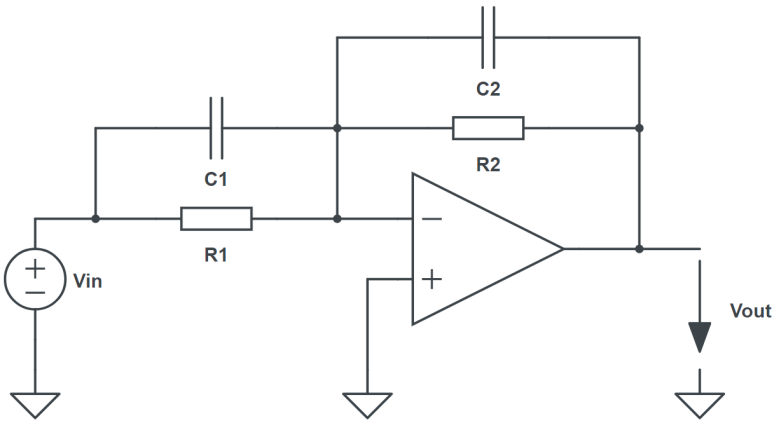

Figure 5.1: Inverting operational amplifier as first order active RC filter

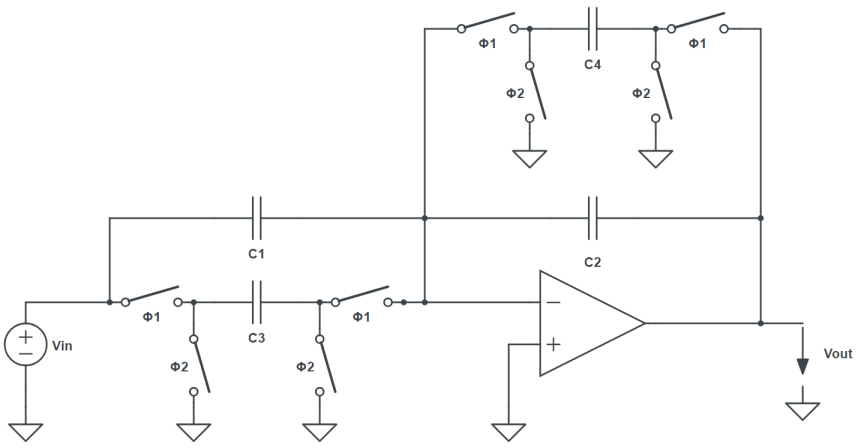

Figure 5.2: Inverting operational amplifier as first order switched capacitors filter

Out of the mentioned implementations most suitable for this application seems to be the active RC filter and last implementation utilizing switched capacitors and capacitor matrixes, especially because they have constant DC gain.

5.1 Comparison of chosen compensating circuit implementations

To determine which of the two chosen implementations is more suitable and has better performance simulations in Cadence Virtuoso were run. Both implementations are tested on compensating transfer function of the notch with dimensions of 8x5 mm and air gap 1.5 mm. The ideal compensation found in Matlab is simulated by using ideal source which has pole and zero as its parameters. In this case pole is ω_p = -26826.86 s^{-1} and zero is ω_z = -12169.38 s^{-1}. Each of these two implementations simulates how reliably it can reproduce the ideal transfer function and most importantly how consistent it is with changes in temperature and process variations. For this purpose, simulation in corners is used.

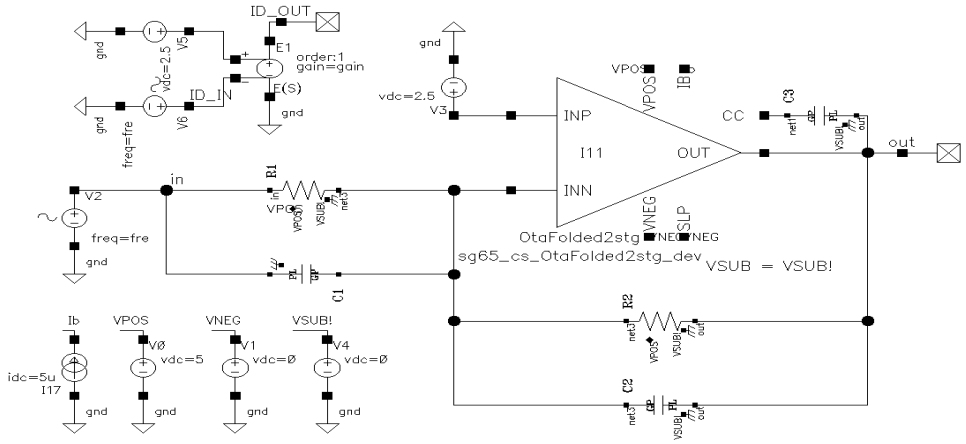

Figure 5.3: Simulated active RC filter

In Figure 5.3 is a simulated circuit of active RC filter. In the top left corner is the ideal source generating the ideal compensating function from Matlab. The circuit in Figure 5.3 is equivalent to the one in Figure 5.1 and it uses real components. Both resistors have value of 10 MΩ, C_1 = 8.23 pF and C_2 = 3.73 pF. AC analysis of the circuit is simulated in 40 corners with various process parameters deviations on temperatures -40 °C and 165 °C. The resulting tranfer functions are in Figure 5.4. It is apparent that the spread of the transfer functions is significant and cannot satisfy given constrains of 2 % error in magnitude and 1° of phase shift up to 3 kHz. In Table 5.1 are absolute values of maximal deviation from ideal compensation on interval up to 3 kHz. In nominal conditions results are within given constrains, however out of 40 runs in corners only one pasess. Moreover mean and maximal values of deviations are well over constraining values.

Simulated circuit of switched capacitors filter, which is equivalent to circuit in Figure 5.3 is in Figure 5.5. This circuit undergoes the simulations as the previous one, but as it is switched circuit instead of AC analysis PAC analysis has to be used. Capacitors C_1 and C_2 stay the same as in the previous circuit

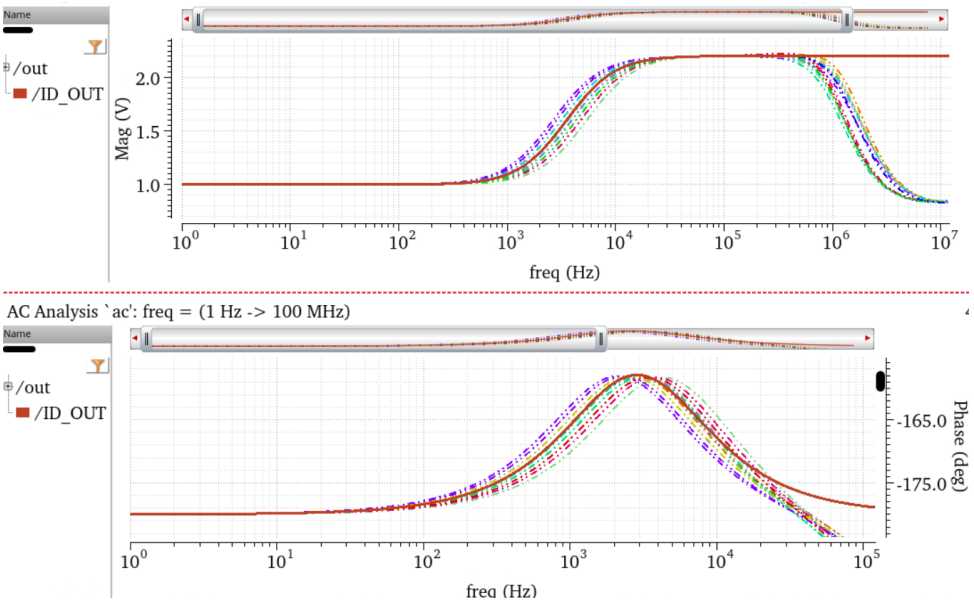

Figure 5.4: Trasfer functions of active RC filter simulations in corners

	Constrains	Nominal	Mean	Maximal
Magnitude	2 %	0.57 %	8.78 %	21.69 %
Phase shift	1°	0.24°	1.74°	4.68°

Table 5.1: Active RC filter implementation transfer function deviations up to 3kHz from ideal transfer function

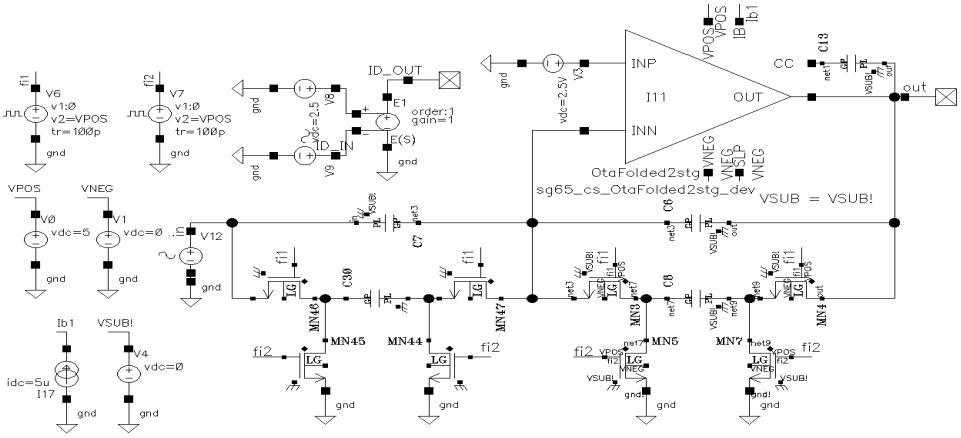

Figure 5.5: Simulated switched capacitors filter

and resistor are replaced by switched capacitors with capacitance of 50 fF and switching frequency of 2 MHz what results in equivalent resistance of 10 MΩ. Graph of the transfer functions in corners of realization with switched capacitors is in Figure 5.6 and results are in Table 5.2. It is apparent that this realization is much more consistent. The transfer functions in Figure 5.6 hold tightly together in comparison to ones in Figure 5.4. Also the deviation

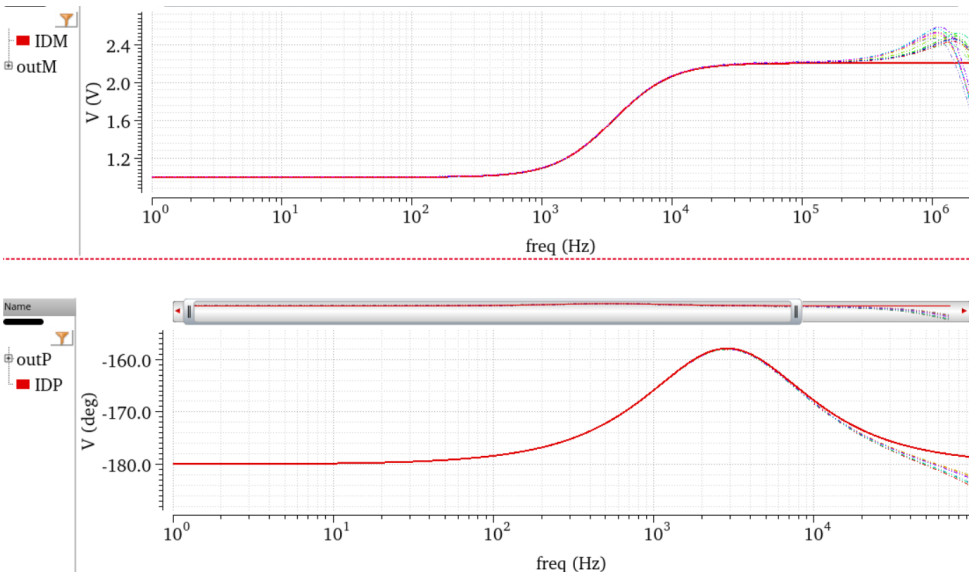

Figure 5.6: Trasfer functions of switched capacitors filter simulations in corners

values listed in Table 5.2 are much smaller, moreover they satisfy all the requirements in all corners.

The results are unequivocal and the implementation with switched capacitors exceedes the active RC implementation, therefore it is the one chosen to be designed for application in this thesis.

	Constrains	Nominal	Mean	Maximal
Magnitude	2 %	0.63 %	0.69 %	0.86 %
Phase shift	1°	0.14°	0.15°	0.21°

Table 5.2: Switched capacitors filter implementation transfer function deviations up to 3kHz from ideal transfer function

Chapter 6

Design of equalizer circuit cells

This chapter documents the design flow of compensating circuit - equalizer. Circuits presented in the previous chapter (Chapter 4), which served for comparison of different implementations, have single ended output. In contrast the designed circuit will have differential output. As was concluded in the Chapter 4 the designed compensation circuit will consist of filter with switched capacitors used as resistors and will be tuned by connecting desired number of elementary capacitors in capacitor matrixes. First step in design is to find values of external components needed to compensate all possible notch transfer functions.

6.1 External components definiton

To get values of external components it is necessary to obtain transfer function of the designed circuit. Transfer function of circuit in Figure 5.1 is Equation 6.1.

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \cdot \frac{1 + sC_1R_1}{1 + sC_2R_2} = -\frac{C_1}{C_2} \cdot \frac{s + \frac{1}{C_1R_1}}{s + \frac{1}{C_2R_2}} \tag{6.1}$$

If Equation 6.1 is compared with general formula first order transfer function with pole and zero in Equation 4.3, it gives following formulas for cutoff frequencies

$$\omega_z = \frac{1}{C_1R_1} \tag{6.2}$$

$$\omega_p = \frac{1}{C_2R_2} \tag{6.3}$$

Also besides pole and zero it is possible to obtain DC gain, Equation 6.4 and gain in infinity, Equation 6.5.

$$H(0) = H_\infty \frac{\omega_z}{\omega_p} = -\frac{R_2}{R_1} \tag{6.4}$$

$$H\infty = -\frac{C_1}{C_2} \tag{6.5}$$

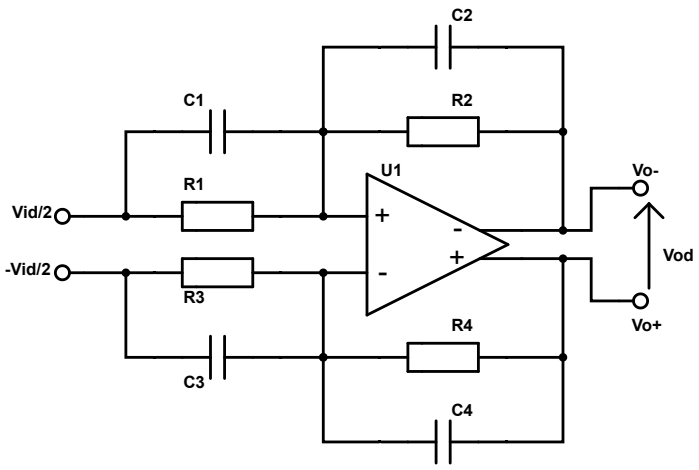

Figure 6.1: Fully differential circuit realization

All formulas above are for circuit from Figure 5.1, however this circuit has single ended output and designed circuit has differential output. This differential output version of the circuit is illustraded in Figure 6.1. For correct behavior of the circuit $R_1 = R_2 = R_3 = R_4$, $C_1 = C_3$, $C_2 = C_4$ is true. Only C_1 and C_2 will be used to refer to all equal components. The transfer function of the circuit with differential output in Figure 6.1 is depicted in Equation 6.6.

$$H_{Diff}(s) = \frac{R_2}{R_1} \cdot \frac{1 + sC_1R_1}{1 + sC_2R_2} = \frac{C_1}{C_2} \cdot \frac{s + \frac{1}{C_1R_1}}{s + \frac{1}{C_2R_2}} \tag{6.6}$$

Unlike transfer function of the single ended circuit transfer function of fully differential circuit from Equation 6.6 is positive, therefore this circuit is noninverting. Due to this fact also Equations 6.4 and 6.5 are positive for fully differential circuit.

From Equations 6.2 to 6.3 it is possible to determine values of external components. As DC gain is required to be invariable and ideally one, all resistors will be equal. As capacitors C_1 and C_2 are composed of matrixes of elementary capacitors Equations 6.2 and 6.3 will be used to determine only the maximal value of each capacitor matrix (C_1, C_2). Maximal values of capacitor matrixes C_1 and C_2 can be obtained by knowing the pole and zero of compensating functions, wich are located on the lowest frequencies. The zero located on the lowest frequency is s_{zl} = -12 161 rad/s and determines value of C_1 by relation in Equation 6.7. This zero corresponds to pole of notch transfer function with dimensions N = 8 mm, T = 5 mm and AG = 1.5 mm. The lowest located compensating function pole corresponds with zero of notch

transfer function with dimensions $N = 8$ mm, $T = 5$ mm and $AG = 3.5$ mm and it is s_{pl} = -16 743 rad/s. This pole determines maximal value of C_2 by Equation 6.8. To determine the values of capacitors, resistor values are also to be chosen. As the capacitor values are desired to be in pF because of integration capabilities. Resistor values will be set in orders of tens of MΩ. Calculations of exact total values of capacitors are in Equations 6.7 and 6.8. Resulting values are $C_1 = 4.11$ pF and $C_2 = 2.986$ pF.

$$C_1 = \frac{1}{\omega_z R} = \frac{1}{12161 \cdot 20 \cdot 10^6} = 4.112 \text{ pF} \tag{6.7}$$

$$C_2 = \frac{1}{\omega_z R} = \frac{1}{16743 \cdot 20 \cdot 10^6} = 2.986 \text{ pF} \tag{6.8}$$

6.2 Design of form of capacitor matrixes

This chapter goes through the process of designing the capacitors matrixes. This means resolving the number, capacity, and its distribution of elementary capacitors for each capacitor matrix.

6.2.1 Determination of capacitor matrixes form

The process of finding the best solution for capacitor matrix composition was driven by the requirement that the number of elementary capacitors must be 2^{n-1} so it can be easily configurable by n control signals. Also to compare geometric and linear distribution of elementary capacitors values on interval up to maximal value determined in Equations 6.7 and 6.8.

The process of finding optimal capacitor matrixes is performed in Matlab simulations. The aim is to find the smallest number of elementary capacitors which can assure compensation for all possible notch transfer functions within given constraints. The first step in this process is generating vector of capacitor values, distributed linearly or geometrically, up to maximums given by Equations 6.7 and 6.8. By combination of capacitor values in these vectors all possible compensating transfer functions are obtained. From these transfer functions the best compensating one is selected for each notch transfer function and maximal error in magnitude and phase on the interval 0-3 kHz caused by discretization of compensation is saved.

These simulations were performed for matrixes with 15 elementary capacitors for both C_1 and C_2. This was far from sufficient compensation using both distributions. The numbers of elementary capacitors were raised several times before the sufficient counts of elementary capacitors were found. The smallest sufficient number of elementary capacitors was 31 for C_1 and 63 for C_2, however these counts were sufficient only for linear distribution. Comparison of compensating abilities of these two distributions is illustrated in Figures 6.2 and 6.3, which show maximal error in magnitude on the interval 0 - 3 kHz caused by discrete number of compensating functions. Both Figures show simulation for $AG = 1.5$ mm as this is the smallest air gap, which has

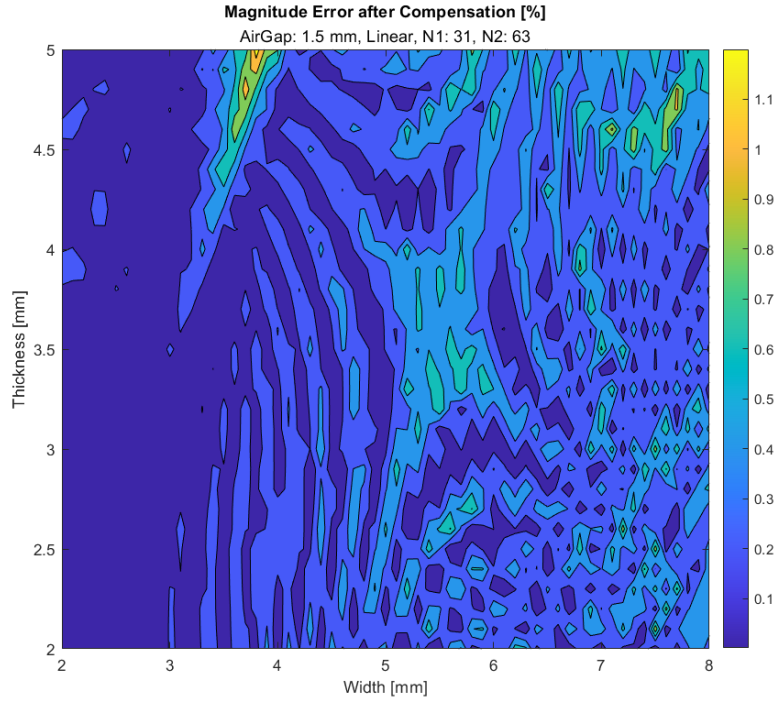

Figure 6.2: Maximal error in magnitude after compensation - linear (up to 3 kHz)

most significant attenuations as was described in Section 2.2. These larger attenuations also led to more difficulties and bigger errors during finding the best discrete compensating transfer functions. Better performance of linearly distributed values of elementary capacitors was expected since in the case of geometric distribution the bigger values of capacitors, used for compensating more significant attenuations, with lower cutoff frequencies, are sparser. This conclusion is also more convenient for chip integration as all elementary capacitors forming matrixes of C_1 will have the same value and all elementary capacitors forming matrixes of C_2 will have the same value. However, the value of elementary capacitors of C_1 differs from those of C_2. Because capacitance of integrated capacitors is constrained by capabilities of the used technology. The values of the elementary capacitors had to be slightly changed to fit values which is possible to implement by used technology. Their capacitances are $C_{el1} = 132.48$ fF for C_1 and $C_{el2} = 47.34$ fF for C_2. This slight changes of elementary capacitors values also resulted in slight change of total capacitances of C_1 an C_2. The total capacitances of C_1 and C_2 matrixes after adjustments caused by technological constrains are $C_1 = 4.107$ pF and $C_2 = 2.982$ pF.

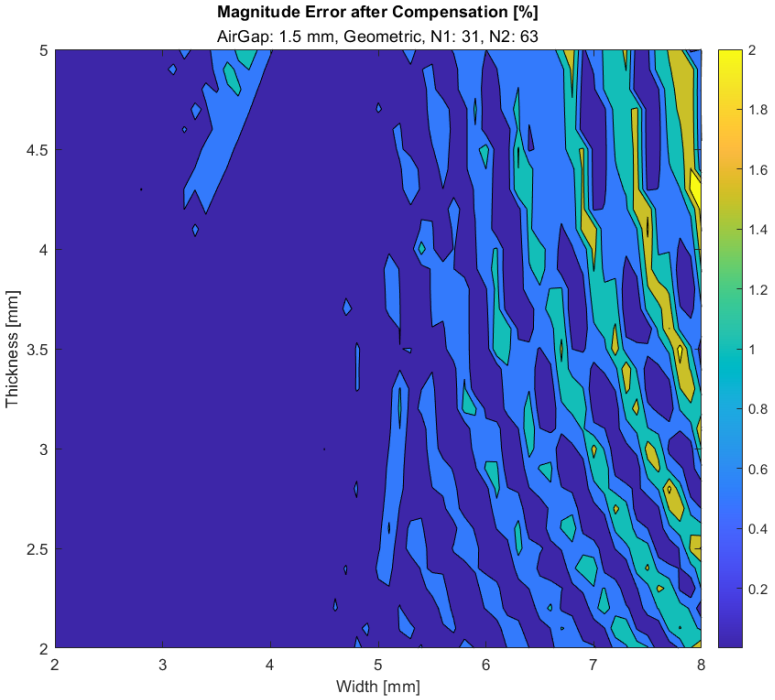

Figure 6.3: Maximal error in magnitude after compensation - geometric (up to 3 kHz)

6.2.2 Circuit implementation

The following list sums up parameters of capacitor matrixes.
Capacitor C_1 matrix:

- Number of elementary capacitors: 31
- Capacitance of one elementary capacitor: $C_{el1} = 132.48$ fF
- Total capacitance of C_1 matrix: $C_1 = 4.107$ pF

Capacitor C_2 matrix:

- Number of elementary capacitors: 63
- Capacitance of one elementary capacitor: $C_{el2} = 47.34$ fF
- Total capacitance of C_2 matrix: $C_2 = 2.982$ pF

In semiconductor technology various types of capacitors are available, such as MIM (Metal-Insulator-Metal), MOM (Metal-Oxide-Metal) or MOS (Metal–Oxide–Semiconductor). Each type of capacitor has its drawbacks and benefits. MIM and MOM capacitors are formed between two metal layers and have lower capacitance per unit area in comparison to MOS capacitors, moreover they require more steps in fabrication process. The advantage of these capacitors is that their capacitance does not change with applied

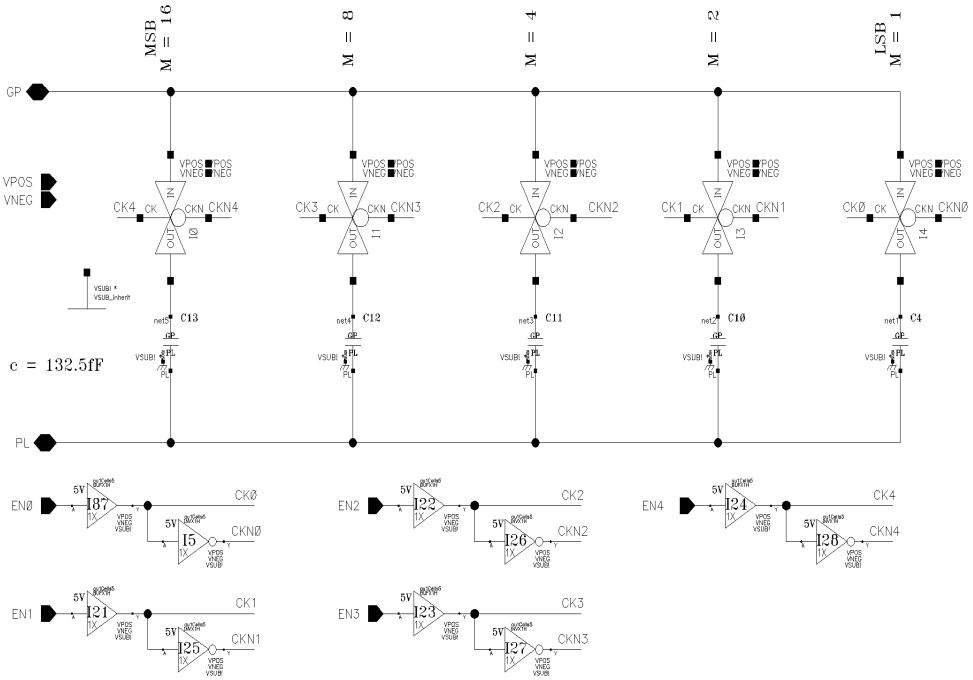

Figure 6.4: Capacitor C_1 matrix schematic

voltage. MOS capacitors have higher capacitance per unit area, however their capacitance varies with applied voltage. [20]

For this design MOS capacitor using polycrystalline silicon instead of metal on its gate was chosen, because of much smaller area requirements and easier implementation. The variability of capacitance of used capacitors was tested to examine whether it may cause noticeable problems in the designed circuit.

In the simulation which tested capacitance variation, voltage was swept from 0 V to ± 5.5 V which is maximal allowed voltage. The variance in capacitance grew with applied voltage difference, however it was quite insignificant. The maximal variation on positive sweep was 0.97 % for 5.5 V, on negative sweep 4.7 % for -5.5 V. These voltages are well above expected applied voltages to these capacitors in the designed circuit, therefore capacitance variations will be also smaller. The maximal expected voltage applied difference to capacitors is ±2.75 V. For these voltages maximal capacitance variation is 0.77 % for 2.75 V and 1.82 % for -2.75 V.

The schematics for capacitor matrixes C_1 and C_2 are in Figures 6.4 and 6.5 respectively. As can be seen in these figures elementary capacitors are connected in five and six parallel branches. The number of elementary capacitors in each branch grows with the power of two. With this connection any number of elementary capacitors from 0 to 31 and 63 can be simply connected to the circuit by switching the transmission gates in each branch. The complete desing of cells of capacitor matrixes is besides elementary capacitors composed of transmission gates, buffers and invertors to assure proper switching of transmissions gates.

This design of capacitors matrixes enables configuration of each capacitor

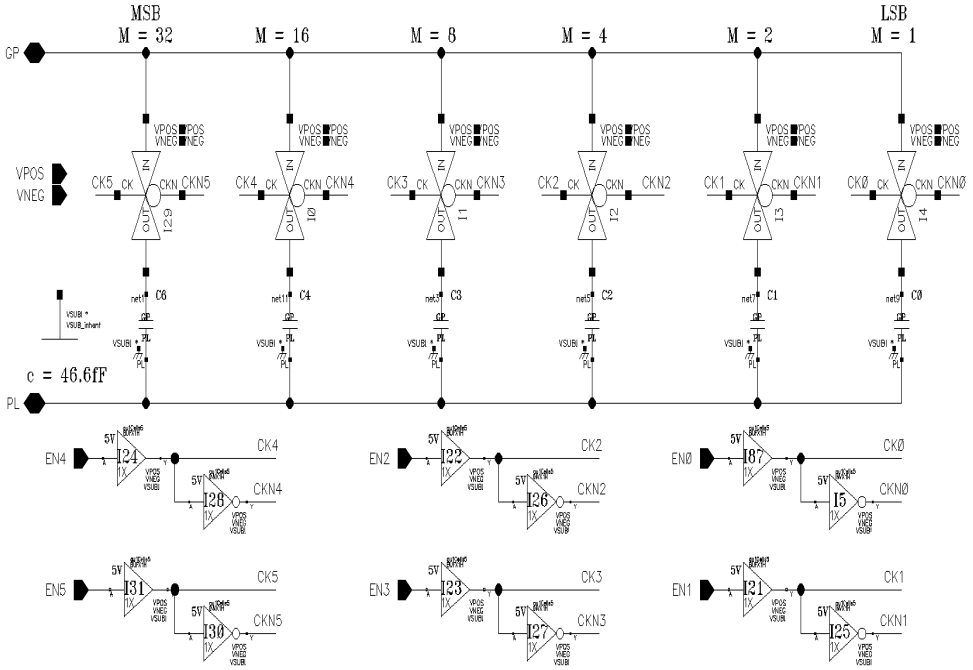

Figure 6.5: Capacitor C_2 matrix schematic

matrix - connecting desired number of elementary capacitors in each matrix to the circuit. The configurations will be described using MC1 for C_1 and MC2 for C_2 to state the number of connected elementary capacitors in each matrix.

6.3 Switched capacitors

In the Section 4.1 implementation using switched capacitors was chosen. This short section goes trough substitution of resistors calculated in Section 5.1 by switched capacitors.

The replacement of resistor with switched capacitor which behaves as it has equivalent resistance as the resistor is quite simple and straightforward. However, several conditions are required. [21] [20]

- Φ_1 and Φ_2 are pair of nonoverlaping clocks.
- Resistor approximation is useful only for frequencies much lower than switchng clock frequency. For moderate and higher frequencies discrete time analysis would be required.

The Figure 6.6 shows the simplest implementation of resistor using switched capacitor. For equivalency in Figure 6.6 conditions above must be fulfilled. If circuit in Figure 6.6a, is analyzed from charge prespective the relation for charge of the capacitor C_1 is given by Equation 6.9. Where Q is charge of the capacitor, C is capacitance of the capacitor and V is voltage across the capacitor. [21] [20]

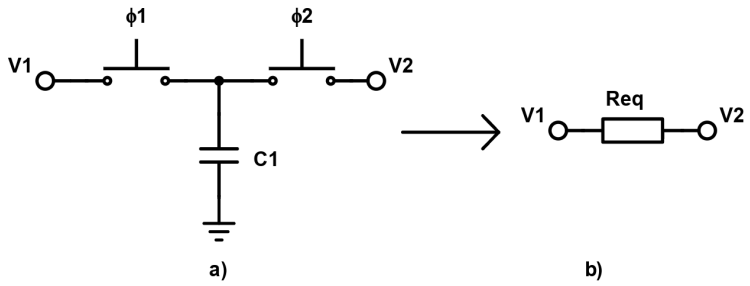

Figure 6.6: Switched capacitor and resistor equivalency

$$Q = CV \tag{6.9}$$

Since C_1 is charged to V_1 and then to V_2 thanks to nonoverlaping clocks Φ_1 and Φ_2 charge ΔQ is transfered through capacitor C_1. As this repeats each clock period charge transfered from V_1 to V_2 over one clock period can be determined as well as equivalent average current. Transfered charge is given by Equation 6.10 and average current by Equation 6.11. T is period of switching clock. Relation for current through the equivalent resistor in Figure 6.6b is given in Equation 6.12. From Equations 6.11 and 6.12 it can be stated that average current through switched capacitor in Figure 6.6a is equivalent to current through resistor in Figure 6.6b if Equation 6.13 is true. [21] [20]

$$\Delta Q = C_1(V_1 - V_2) \tag{6.10}$$

$$I_a = \frac{C_1(V_1 - V_2)}{T} \tag{6.11}$$

$$I_{eq} = \frac{V_1 - V_2}{R_{eq}} \tag{6.12}$$

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \tag{6.13}$$

The Equation 6.13 gives the relation between design parameters of switched capacitor and equivalent resistor. This enables design of switched capacitors in this application as the value of equivalent resistor was determined in Section 5.1. The value of resitors in designed filter is R = 20 MΩ, therefore equivalent resistor R_{eq} for switched capacitors has value of 20 MΩ as well.

There are many possible ratios of switching frequency and capacitance which give value of 20 MΩ from Equation 6.13, but just two of them were chosen as they were reasonable considering technological limits and condition that switching frequency must be much higher than signal frequency.

First considered realization is f_{s1} = 2 MHz and C_{sw1} = 25 fF and second one f_{s2} = 1 MHz and C_{sw2} = 50 fF. These two realizations were tested to

find out wich one gives more consistent results with variations in temperature and technological parameters. This turned out to be the second realization probably because value of 25 fF is almost minimal technological value of used capacitors, for which technological imperfections are more significant. Therefore the resistors in design circuit are implemented using switched capacitors with capacitance 50 fF and switching frequency 1 MHz. Even though it is the lower frequency out of the two considered ones it still satisfies the condition for resistor equivalence as it is ten time higher than maximal frequency for which were run notch simulations and several hundered times more than constrained frequencies.

6.4 Fully differential operational amplifier design

Fully differential operational amplifiers are operational amplifiers that possess not only differential input terminals but also differential output terminals. This type of operational amplifier is sought after in many integrated-circuit applications as it offers numerous advantages over its single-ended counterparts. Thanks to this approach, the output signal swing is increased by a factor of two in comparison to a single-ended implementation. Differential signal processing also has the advantage of canceling common-mode signals and minimizing the influence of clock feedthrough. Because of these advantages, a fully differential implementation was chosen for this application. [20]

Main drawback of fully differential operation amplifiers is that they require additional circuitry to establish common-mode output voltage. This circuitry is called common-mode feedback circuit. Ideally, this circuit should prevent the drift of the output common voltage and maintain it at the desired level. [21]

Conditions	**Min.**	**Typ.**	**Max.**	**Units**
Temperature	-40	25	170	°C
Supply voltage 3.3 V device	3	3.3	3.6	V
Input differential voltage 3.3 V device	-1.75		1.75	V
Common mode reference 3.3 V device		1.5		V
Supply voltage 5 V device	4.5	5	5.5	V
Input differential voltage 5 V device	-2.65		2.65	V
Common mode reference 5 V device		2.25		V
Output load resistance (each output)	64			kΩ
Output load capacitance (each output)	0		1	pF
Design parameters				
Open loop gain	70	80		dB
Phase margin	45	60		°
Offset voltage	-12.6		12.6	mV
Unity Gain Bandwidth	7	10		MHz
Supply current		415	430	µA

Table 6.1: Key parameters of designed operational amplifier

Before proceeding with the design, certain requirements must be specified. First and foremost, designed operational amplifier must be operating on supply voltage ranging from 3 V to 3.6 V and 4.5 V to 5.5 V. Moreover, since this circuit is designed as a part of sensor intended for automotive industry it must meet specific requirements at temperatures ranging from -40 °C to 170 °C. The key requirements and design conditions are detailed in Table 6.1.

6.4.1 Input stage design

In the input stage design, as depicted in Figure 6.7, the biasing current Ib = 5 µA for the operational amplifier is sourced through the mother transistor MN1 and is mirrored by MN2, MP3, and MP4 in a 1:1 ratio. Transistor MP4 supplies the input differential pair composed of transistors MP1 and MP2 by tail current equivalent to biasing current Ib. Transistor MN6, placed above MN2, to cancel the influence of channel length modulation caused by large drain-to-source voltage, which would otherwise lead to an increase in the mirrored current.

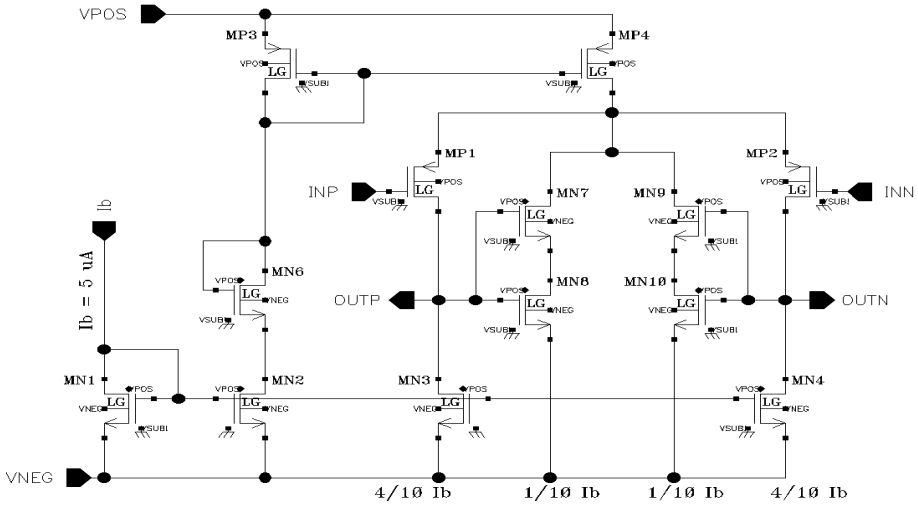

Figure 6.7: Input stage of designed fully diferrential operational amplifier

As common-mode voltage is set below the half of the supply voltage and therefore differential signals referenced to this common-mode level get closer to $VNEG$ than to $VPOS$. PMOS differential pair were chosen for this design, since PMOS transistors can process signals close to $VNEG$ potential, which is problematic with NMOS transistors. Transistors MN3 and MN4 act as active load for differential pair and are designed to mirror 40 % of bias current each. This leaves 20 % of bias current to flow through transistors MN7-MN10 in Figure 6.7.

Transistors MN7-MN10 in Figure 6.7 are used as common-mode feedback for the first stage. The connection of these transistors, with the lower transistors operating in the triode region, is used because if MN7, MN8 and MN9, MN10 have the same dimensions, which they have, the connection is equivalent to a transistor with half the $\frac{W}{L}$ ratio - twice of the length of single transistor.

The circuit operates as follows: any change in common-mode voltage at the inputs causes minor voltage change of the voltage at the outputs. This change also changes V_{GS} of MN7 and MN8 which leads to variations in their drain currents. Since the tail current is fixed to a certain value, any discrepancy in the drain currents of MN7 and MN8 is forced to differential pair where it opposes previous change in output voltage.

6.4.2 Second stage and common mode feedback circuit design

Figure 6.9 shows the design of the entire operational amplifier. The second stage is constructed using NMOS transistors (MN11, MN12) configured with common source and PMOS transistors (MP5, MP6) as active load. This operational amplifier is designed with two stages, like most multistage amplifiers, because it can provide high gain. However, the problem of two stage amplifiers is that these amplifiers have transfer function with two poles which are at relatively high frequencies and close to each other. Without proper compensation, these amplifiers tend to be unstable, potentially leading to oscillations or the clamping of the amplifier's output to one of the supply voltages. [20]

The requirement for stability is that the gain characteristics of amplifier's magnitude frequency characteristic crosses 0 dB point before its phase characteristic reaches 0°. The measure given by the value of the phase when magnitude characteristic is 0 dB is called phase margin and its desired value is at least 45°. [20]

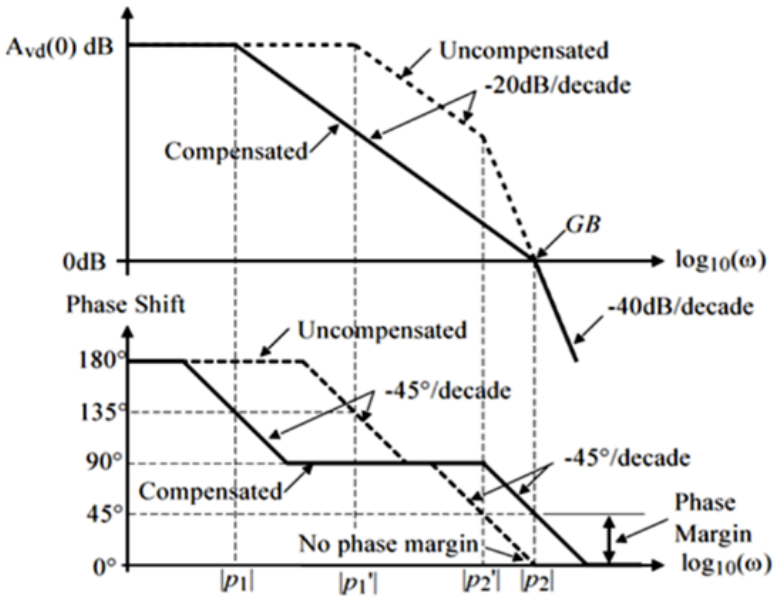

Figure 6.8: Effect of Miller compensation on two stage amplifier transfer function [O5]

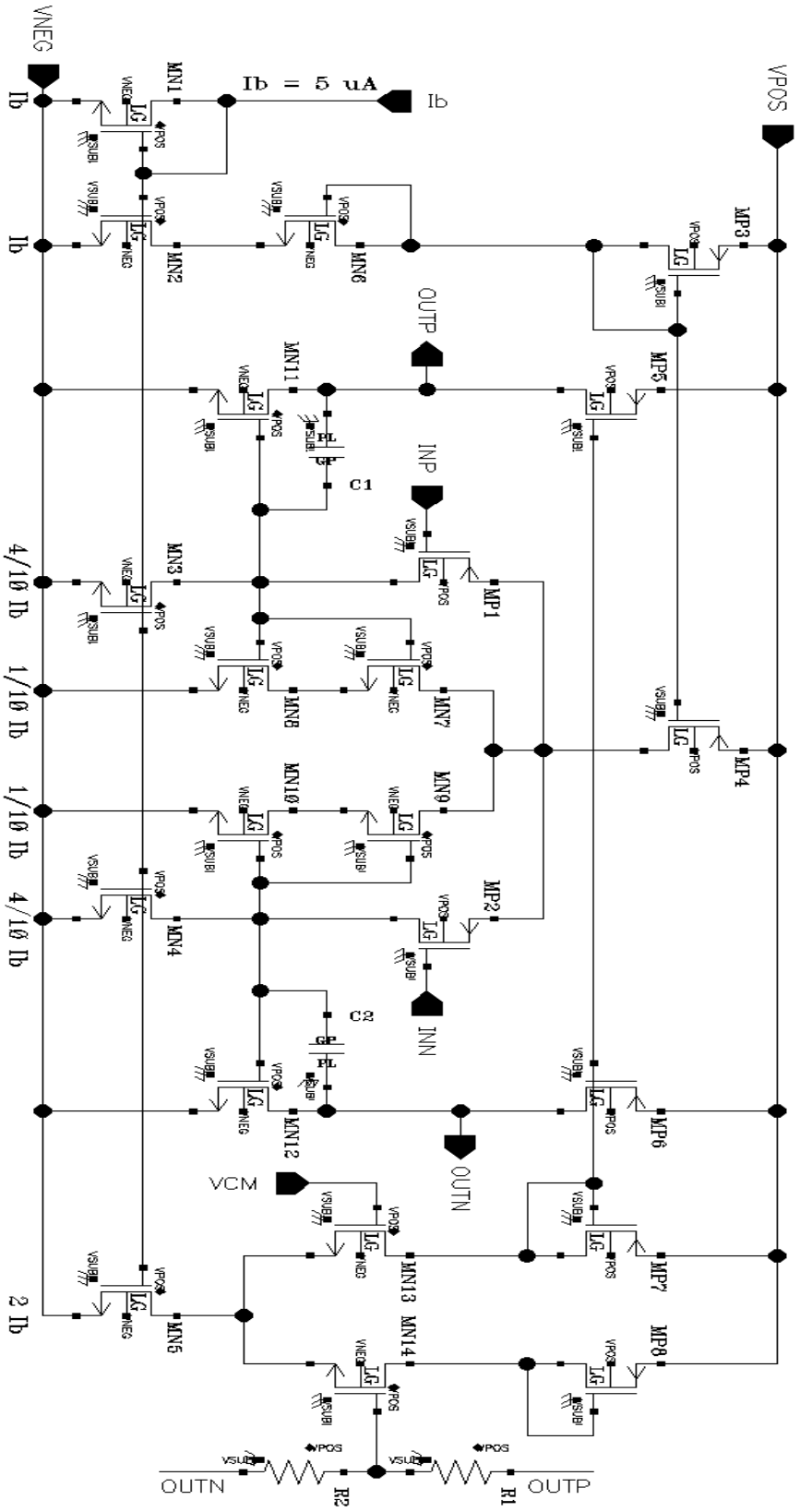

Figure 6.9: Fully differantial operational amplifier structure

To reach the required phase margin and ensure stability of operational amplifier, compensation is needed. In this design, the Miller compensation technique is employed. This technique is applied by connecting capacitor from the output to the input of the second stage. This technique leverages the Miller theorem to change positions of the poles. The usage of the compensation capacitor moves the first stage pole closer to the origin of complex frequency plane (to lower frequencies) and second stage pole away from the origin of the complex frequency plane (to the higher frequencies). The first stage pole is called "Miller's pole" and it is dominant. Second pole is called "output pole" and it is strongly dependent on the load capacitance. The relocation of the poles resulting in incrase of the pahse margin is ilustrated in Figure 6.8. However, this compensation also introduces right-half plane zero located on the real axis. This zero limits the achievable bandwidth of the amplifier. If the bandwidth of the designed amplifier will not be sufficient the additional advanced techniques will have to be used to overcome this drawback. [20]

In this design, two compensating capacitors (C_1, C_2) are used-one for each differential branch. The composite of transistors MN7-MN10 in the first stage has the same V_{GS} as amplifying transistors of second stage MN11 and MN12. Consequently, their drain currents are set by the $\frac{W}{L}$ ratios. That's the reason behind using transistors MN7-MN10 this connection, because with this connection larger drain currents trough MN11 and MN12 and higher gain can be obtained with smaller silicon area in comparison to use of single transistor in their place.

When fully differential operational amplifier is connected in with feedback loop, circuitry used to stabilize the output common-mode voltage is required. In this design shown in Figure 6.9 common-mode feedback circuitry is at the bottom of the page.

The CMFB (common-mode feedback) consists of one-stage differential amplifier. One input is connected to voltage reference (V_{CM}), while the other to voltage divider realized by resistors R1 and R2 connected to outputs of the operational amplifier. If common-mode voltage on the outputs drifts from the level equal to V_{CM} this change propagates to the gate of MN14 causing change in its drain current. Opposite change in current through MN13 occurs as the total current is set by MN5. MP7 and MN13 have identical drain currents currents therefore. MP7 mirrors its current to MP6 and MP5, therefore the change in MP7 also propagates to MP5 and MP7 where it opposes the change in output voltage and whole loop is stabilized on common mode voltage equal to V_{CM}.

6.4.3 Verification of operational design parameters

The initial step in verification of the designed operational amplifier was to confirm that all transistors intended to be in saturation are saturated. This condition was verified using Monte Carlo (MC) simulations across nominal, minimal, and maximal supply voltages, as specified in Table 6.1. Additionally, these simulations were conducted at temperatures of -40 °C, 25 °C, and 170 °C. All simulations passed, with all transistors remaining in saturation

under every tested condition.

Subsequently, the design verification process involved assessing whether the operational amplifier met the parameters outlined in Table 6.1. For this purpose, stability simulations were performed. Stability simulations are performed not only on differential loop, but as fully differential operational amplifiers also have common mode feedback loop to stabilize common mode voltage on its outputs, stability of this loop must be verified too. The circuit schematic used for stability analysis is presented in Figure 6.10. Probe I6 visible in Figure 6.10 is used for stability analysis of differential loop, however probe for common mode feedback loop is placed inside the operational amplifier between resistors R1, R2 and gate terminal of MN14 in Figure 6.9. In Figure 6.10 it can be seen that simulation was run with maximal values of load capacitors and minimal values of load resistors. This load setup was chosen as worst case because of output pole dependency on load capacitance.

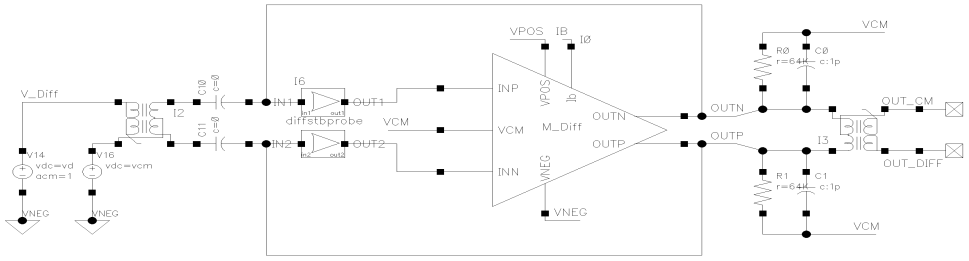

Figure 6.10: Schematic of circuit used for stability analysis

Stability simulation gives results of differential open loop gain, differential phase margin and unity gain bandwidth (UBW). At first the simulation was run for all supply voltages from Table 6.1 in nominal corner. Differential DC open loop gain values are between 83.23 dB – 86.3 dB. Phase margin values are 65.41 – 66.3 and UBW values are between 13.37 – 14.05 MHz. All these values satisfy requirements from Table 6.1 with margin. Common mode DC gain is around 30 dB and phase margin results are more than 110° with UBW approximately 3 MHz. All these results had higher values with higher supply voltage, therefore the designed operational amplifier performs slightly better in 5 V devices than in 3.3 V ones. With results from nominal simulation satisfying the requirements corners and Monte Carlo simulations were run in the same manner as before.

The waveforms from stability analysis in corners at temperatures -40 °C and 170 °C of the differential loop are illustrated in Figure 6.11. On the left side of Figure 6.11, the gain frequency characteristic waveforms are displayed. As can be seen, they correspond with DC gains stated above. The division of the waveforms to several bundles is also apparent. This separation occurs because corner analysis is performed at the two temperature extremes: -40 °C and 170 °C. Waveforms with smaller DC gain are associated with corners with at t = 170 °C, while those with higher DC gain are associated with corners at t = -40 °C. The nominal corners at t = 25 °C are in the midle.

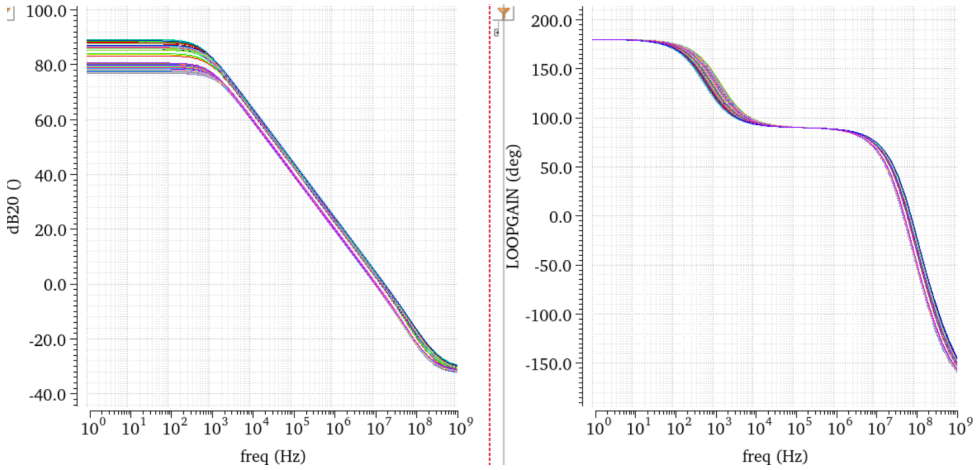

Figure 6.11: Results of stability analysis simulated in corners at temperatures -40 °C and 170 °C

For this characteristics the changes in supply voltage and other technological parameters have much smaller effect compared to the impact of temperature. Although corners at t = 170 °C have smaller DC gain, their cutoff frequency is slightly higher - on average, by a few hundred Hertz. This observation is further supported by the phase characteristisc, as the waveforms of the corners at t = -40 °C are positioned on the lower side of the bundle during the initial descent on the phase graph.

Parameter	Min.	Max.	Mean	Req.	Units
DC Open loop gain	74.35	90.1	83.61	> 70	dB
Phase margin	57.28	69.43	65.87	> 45	°
UBW	9.48	18.23	13.59	> 7	MHz

Table 6.2: Result summary of Monte Carlo stability analysis - Defferential loop

Summarized results of the Monte Carlo simulations for differential loop are stated in Table 6.2. The Monte Carlo simulations were performed with variation in both mismatch and process parameters in 200 points. These simulation results align with the previous findings. However, in comparison to corner simulations, minimal and maximal values are significantly apart from each other. Both trends discovered above were visible in these simulations as well, therefore the minimal value of DC gain was obtained from simulation with a supply voltage of 3 V and temperature of 170 °C while maximal value from simulation with a supply voltage of 5.5 V and temperature of -40 °C. For the phase margin, the lowest one was obtained from MC simulation with a supply voltage of 3 V and temperature of -40 °C while the highest phase margin was obtained from MC simulation with a supply voltage of 5.5 V and temperature of 170 °C. Lastly, the unity gain frequency ranges from 9.48 MHz to 18.23 MHz. Its minimal and maximal values were obtained in corresponding corners with the same conditions as the ones of DC open loop gain.

Summarized results of common mode loop Monte Carlo simulations are in Table 6.3. From these results, it is apparent that the common mode loop is stable under any conditions and possesses a great margin to the border phase margin value of 45°. The gain of this loop is also sufficient as this loop does not require as much gain as the differential one.

Parameter	Min.	Max.	Mean	Units
DC Open loop gain	27.27	35.81	35.48	dB
Phase margin	103.3	116.8	110.7	°
UBW	2.46	5.03	3.61	MHz

Table 6.3: Result summary of Monte Carlo stability analysis - Common monde loop

From the parameters given by Table 6.1 offset and current consumption remain to verify. These parameters were simulated using DC analysis. As for the previous parameters Monte Carlo simulations were performed. The results of these simulations are in Table 6.4.

Parameter	Min.	Max.	Mean	Req.	Units
Offset	-5.89	5.44	0.02	$<\lvert\pm 12.6\rvert$	mV
Supply current	81.69	185.6	141.5	< 430	µA

Table 6.4: Result summary of Monte Carlo stability analysis - Offset and supply current

Both parameters also meet the requirements. An especially good result is the supply current having a mean value of less than one-third of the maximum allowed.

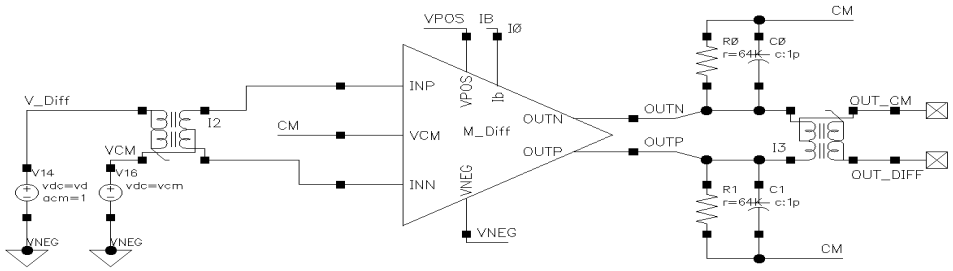

Figure 6.12: Schematic of circuit used for CMRR and PSRR analysis

With these simulations, all required parameters were verified. However, before proceeding with the design of the equalizer, two additional parameters of the operational amplifier were also verified. Those parameters are the common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). The circuit for simulating CMRR and PSRR is depicted in Figure 6.12. These parameters were obtained by running XF analysis which calculates the frequency response from every independent source in the circuit to a designated output. Common-mode rejection ratio was then determined by plugging in frequency responses to the source of common mode signal and

source of differential signal to Equation 6.14. Only corner simulations of these parameters were performed on six supply voltages from Table 6.1. The resulting waveforms of CMRR are shown in Figure 6.13. As can be seen in this figure, DC values of CMRR vary between 114 dB and 132 dB. This variability is mainly caused by variability in differential gain illustrated in Figure 6.11. The CMRR remains above 100 dB until 7.5 kHz in the worst-case scenario, and for nominal conditions, it extends up to 13.23 kHz for a 3.3 V supply voltage and 16.14 kHz for a 5 V supply voltage. At a frequency of 1 MHz, the worst-case CMRR value is 49.32 dB.

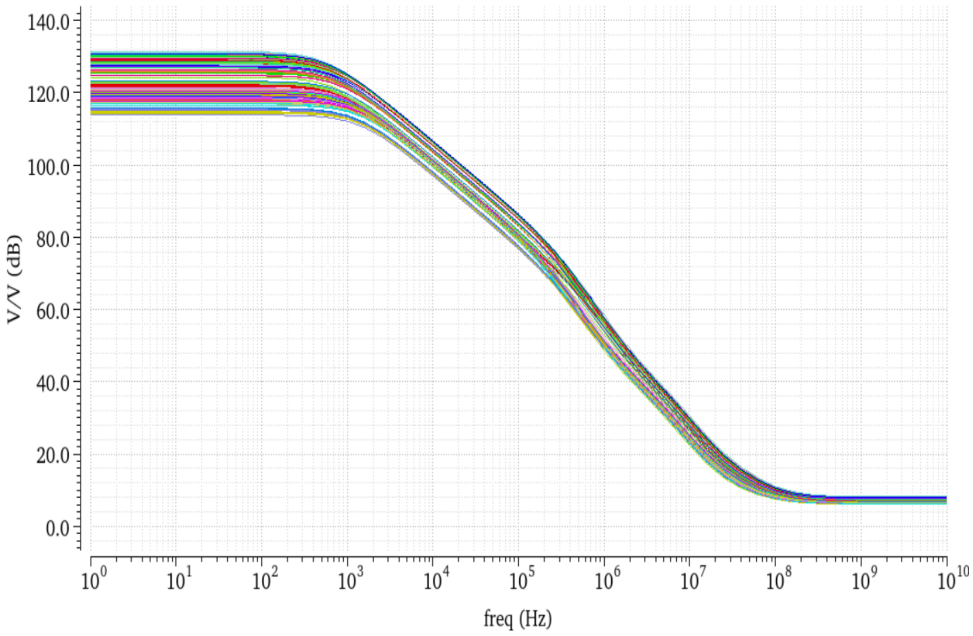

Figure 6.13: CMRR waveforms from corner simulation at temperatures -40 °C and 170 °C

To obtain the PSRR frequency response of the common-mode source constituted to Equation 6.14 was replaced by the frequency response of the power supply source. The resulting waveforms are shown in Figure 6.14. DC and low-frequency values are very similar to CMRR values, however, the descent of PSRR characteristics is steeper, therefore PSRR has slightly lower values on higher frequencies than CMRR. Under nominal conditions on 1 MHz frequency the value of PSRR is 10 dB smaller than CMRR.

$$CMRR(\text{dB}) = 20log\left|\frac{A_{Diff}}{A_{CM}}\right| \tag{6.14}$$

Since the fully differential operational amplifier was the last designed cell and all its parameters exceeded the required values the next step in the design can be taken. That means assembling an entire equalizer using cells and components designed in this chapter.

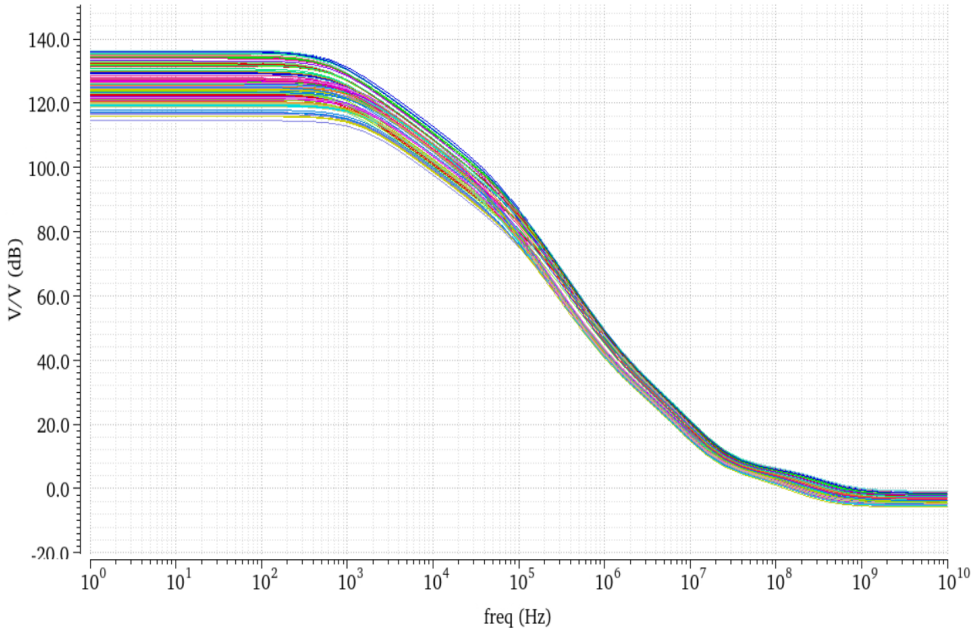

Figure 6.14: PSRR waveforms from corner simulation at temperatures -40 °C and 170 °C

Chapter 7

Equalizer circuit design

With all blocks now designed, the final circuit and its testing can be performed. The circuit combines the ideal circuits illustrated in Figure 6.1, which shows the fully differential implementation of the compensating filter circuit, with the circuit in Figure 5.2, where the resistors of the filter are implemented using switched capacitors. This chapter goes through the design of the final equalizer circuit from the initial design based on the two figures mentioned to its final form with some adjustments and results evaluation.

7.1 Initial equalizer design

The first equalizer circuit assembled from the designed cells, which is a combination of the ideal circuits illustrated in Figure 6.1 and 5.2 is shown in Figure 7.1. In this figure, sources of supply voltages, bias current, and clock sources are omitted, as are the sources for the simulation of ideal frequency characteristic and configuration of capacitor matrixes. These elements are excluded to reduce clutter in the illustration. As shown in Figure 7.1, the ideal switches from Figure 5.2 are implemented using NMOS transistors as it is the simplest implementation with the smallest demand for silicon area. The dimensions of the NMOS switches are minimized according to the capabilities of the technology used. That is because of the clock feed-through, which is dependent on the size of gate capacitance. Smaller gate area results in reduced gate capacitance, thereby diminishing the influence of clock feed-through. The issue of clock feed-through will be explored in greater depth later in the text.

Using only NMOS transistors as switches can pose significant drawbacks. The first issue is that the maximal output signal level is given by $VPOS$ - V_{th}, where V_{th} represents the threshold voltage of NMOS the transistor. When the input voltage of the NMOS switch is close to the $VPOS$ voltage, the output voltage rises slowly because of decreasing V_{GS} of the NMOS. This decrease in V_{GS} leads to an increase in channel resistance. Consequently, with higher channel resistance the value of RC time constant formed by this channel resistance and switched capacitor is larger. Therefore the time required to charge the capacitor is longer and in some cases the switched capacitor can be charged insufficiently.

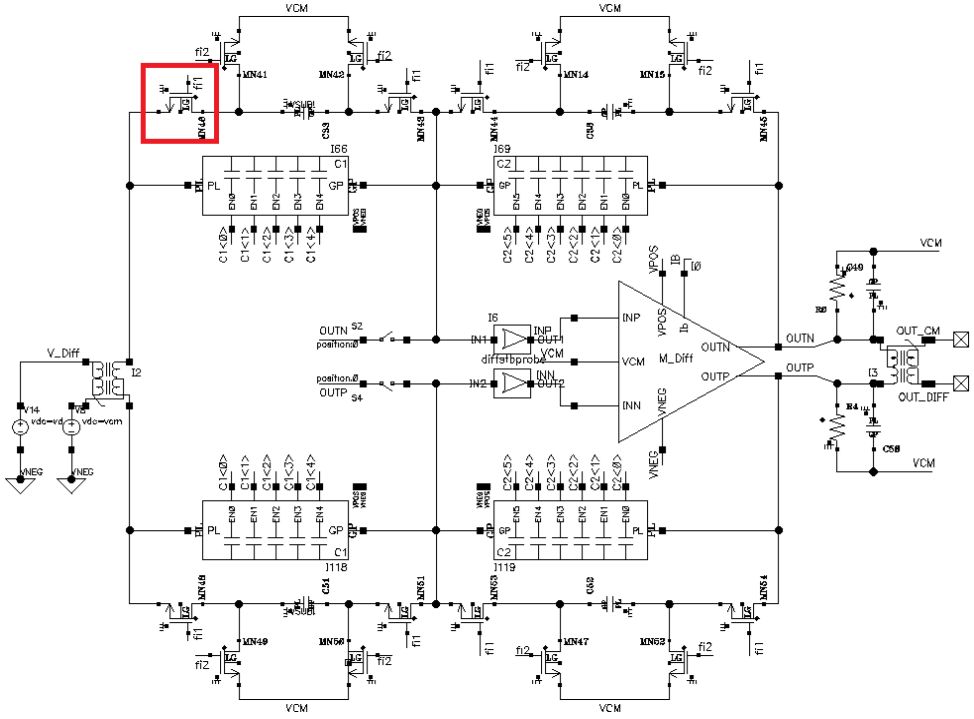

Figure 7.1: Initial equalizer circuit design schematic

Figure 7.2 displays the waveforms of the voltages on transistor in the red square from Figure 7.1. These waveforms confirm claims made in the previous paragraph. Notably, the output waveform with an input differential voltage set to 2.75 V, exhibits a slow rise, and the output voltage does not reach the level of the input voltage. The final voltage value of the purple waveform is the corresponds to the value of $VPOS - V_{th}$. This simulation was done for 5 V device, however the supply voltage was set to 4.5 V. For devices with a supply voltage of 3.3 V, this issue would be even more pronounced.

Before considering alternative implementations, the influence of this phenomenon for the equalizer's frequency responses should be tested. To test the influence of NMOS switches to transfer function, PAC analysis can be performed on the circuit. This simulation is performed with 3.3 V supply voltage. The configuration of the elementary capacitors tuning the frequency responses is MC1 = 31 for capacitor C_1 and MC2 = 39 for capacitor C_2. This configuration compensates for the high attenuations of notch with large dimensions. The resulting frequency response of the equalizer is then compared to the corresponding frequency response of ideal source. The maximal deviations of the equalizers frequency response, with various input differential voltages, are evaluated over the frequency range up to 3 kHz. The results are presented in Table 7.1.

From the results Table 7.1, it is clear that using only NMOS transistors as switches is insufficient. The maximal differential input voltage is 1.75 V, and the large errors of the frequency response occur even with a differential input voltage of 1.5 V.

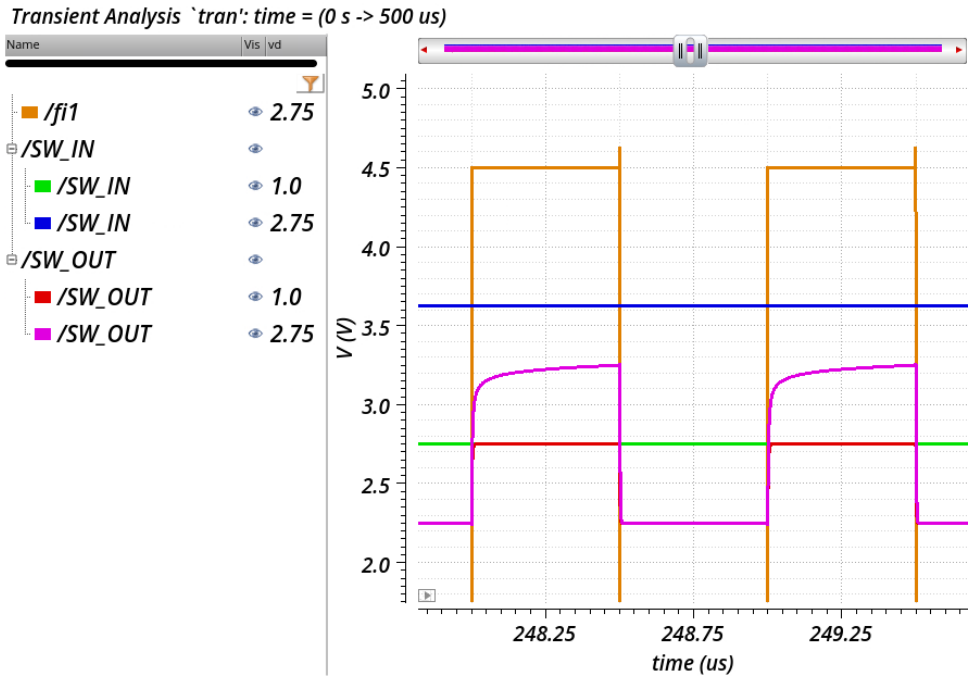

Figure 7.2: NMOS switch waveforms for various input voltages

Input diff. voltage	Magnitude dev.	Phase dev.
0.5 V	0.070 %	0.164°
0.75 V	0.075 %	0.163°
1 V	0.087 %	0.161°
1.25 V	0.186 %	0.133°
1.5 V	20.051 %	6.404°
1.75 V	21.649 %	6.935°

Table 7.1: Transfer function deviation up to 3 kHz for various input voltages

To overcome the complications of switch using only NMOS transistor, switch using NMOS and PMOS transistors in parallel, with their gates connected to opposite control signals can be used instead. This switch is known as a transmission gate. In this connection PMOS supplies the necessary current to the capacitor when NMOS is turning off and NMOS supplies current when PMOS is turning off. The overall equivalent resistance of the transmission gate is consistent over range of input voltage. The schematic of typical transmission gate is in Figure 7.3a. The transistor sizes are kept as small as possible within the given technology to mitigate clock feed-through effects, as mentioned earlier. Another approach to reduce the clock feed-through is illustrated in the Figure 7.3b. Each switched transistor is surrounded by the transistors of the same type, but these additional transistors have half the gate area. Their source and drain are connected, and their switching signal is opposite to the main transistor. These transistors compensate for the charge injected to the gates of main transistors, therefore diminishing the

clock feed-through effect. This application in comparison to the one from Figure 7.3a adds four more transistors to the circuit of each transmission gate, therefore it is appropriate test if this more complicated implementation offers better performance.

The suitability of the transmission gate was evaluated on the equalizer circuit's frequency response, similar to the case of NMOS switches. The resulting frequency responses were similar, however the simpler implementation from Figure 7.3a performed slightly better. Thanks to better performance and simpler design this transmission gate was chosen to replace the NMOS switches. It is also important to note that vertically oriented switches in Figure 7.1 have their drain connected to common mode reference, therefore their V_{GS} remains the same, thus they do not require replacement.

Furthermore, another improvement related to the switches in the circuit in Figure 7.1, can be made by reconsidering their connections. It is evident that the two switches in each feedback loop, connecting the switched capacitors to the inputs of the operational amplifier, are redundant. The same redundancy applies to the inner switches between capacitors and the common mode reference. By optimizing the connections, the total number of switches needed in one feedback loop can be reduced from eight to six.

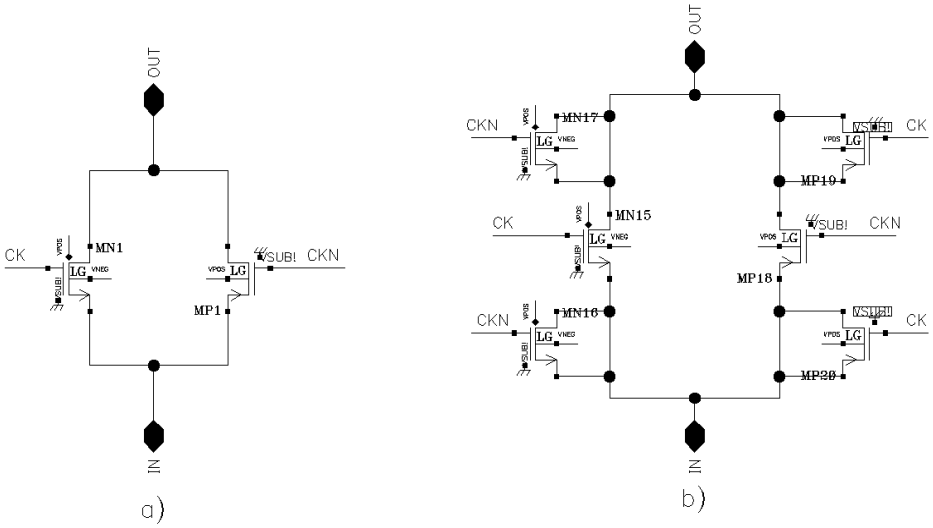

Figure 7.3: Transmission gates schematics

7.2 Improved equalizer design

The new design shown in Figure 7.4 eliminates redundant switches, and NMOS switches have been replaced where necessary. As well as in the case of initial design sources for running simulations are left out in the figure. This improved design will undergo verification to find out if it achieves the aims of this thesis, specifically assessing its ability to compensate for notch frequency responses.

System parameters can be significantly affected by variations in number of connected elementary capacitors to the circuit, which are used to compensate for various notch frequency responses. Testing all possible capacitor variations under all conditions is extremely time-consuming and almost impossible to verify. Additionally, many of the possible configurations are not used. Therefore, it is essential to reduce the number of combinations to relevant ones.

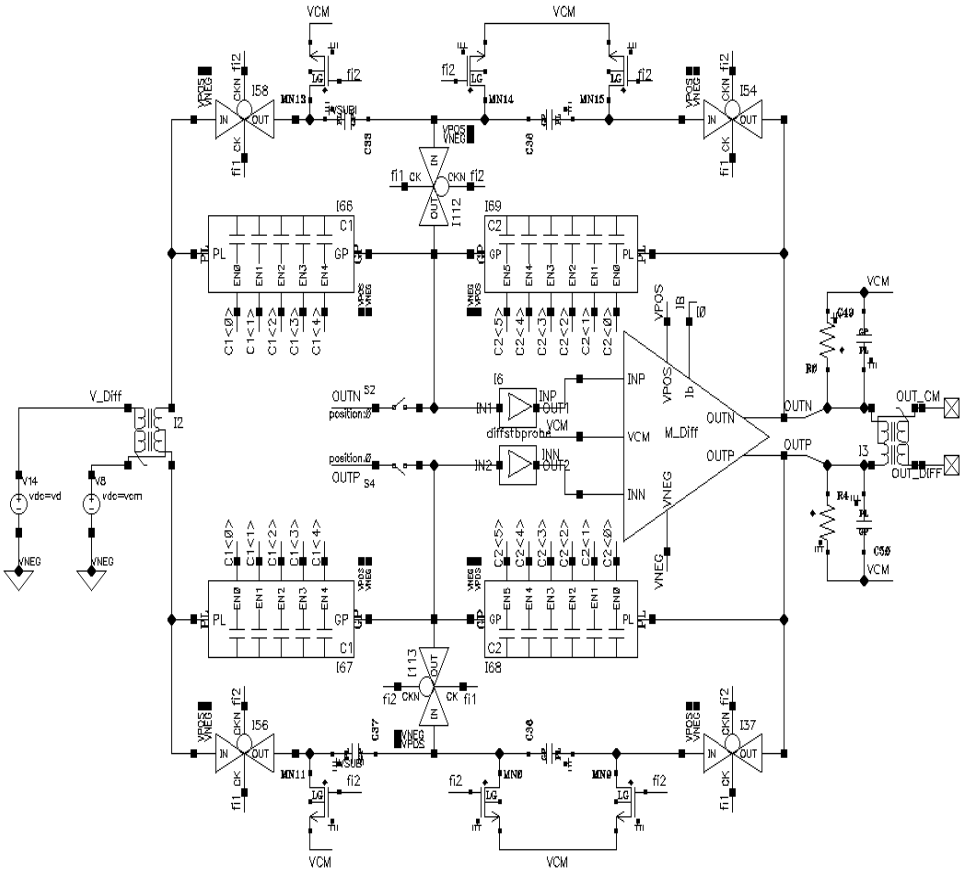

Figure 7.4: Improved equalizer design

In Section 6.4.2, it was stated, that the load capacitance of the operational amplifier significantly influences its stability. Consequently, feedback capacitors have a big influence on the circuit stability. The stability of the circuit is the first factor that undergoes verification.

To reduce the number of capacitor combinations, data form simulations in Section 6.2.1 were utilized. In that section simulations to find the smallest sufficient number of elementary capacitors needed for compensation of all possible notch frequency responses were run. The best compensation from the discrete number of compensating frequency responses was obtained for each notch frequency response. From all of these compensating frequency responses it was determined that 639 unique capacitor combinations are required to compensate for all notch frequency responses. For these combinations stability

simulation in nominal conditions was run. The lowest phase margin was 58.5°, which is well above the threshold of 45°. Generally, the smallest phase margins occurred in combinations where feedback capacitor C_2 had a larger connected capacitance than capacitor C_1, and vice versa. This behavior aligns with the information presented in Section 6.4.2.

The worst performing configurations with other configurations representing general applications and other extremes were tested by Worst-case Monte Carlo.

In this thesis "Worst-case Monte Carlo" will be name for series of Monte Carlo simulations with discrepancies both in process and mismatch, and these Monte Carlo simulations are run on temperatures and supply voltage levels from Table 6.1, with maximal input voltage specified in the same table. This Worst-case Monte Carlo covers all possible worst case scenarios in specified requirements.

The worst-case results of the Worst-case Monte Carlo simulations of most problematic capacitor combinations are in Table 7.2. First two colums state the number of connected elementary capacitors in C_1 (MC1) and C_2 (MC2) respectively and the thirs states worst case phase margin.

MC1	**MC2**	**Phase Margin**
10	32	45.79°
11	35	46.77°
13	40	48.39°
15	45	49.17°
14	43	49.18°

Table 7.2: Worst case stability results

As Table 7.2 states even in the worst cases is the stability of the circuit above the treshold of 45°. However, most of the combinations have C_1 with larger total conected capacitance than C_2, therefore, the stability is above 60° in all cases.

Alongside the stability simulations also offset and total supply current were evaluated and simillarly as in the case of simulations of operational amplifier they were in all cases of Worst case Monte Carlo simulation well below the maximal limit.

Another important parameter of the circuit to consider is its response time. In this application response time is specified as the time between moment when input reaches 90 % of its final value and the moment when the output reaches 90 % of its final value. This is simulated using transient analysis. On the differential inputs square wave with amplitude of maximal differential input voltage is applied. The waveforms illustrating the response time of the circuit with supply voltage of 5 V are shown in Figure 7.5. As can be seen in the figure the response time on rising edge is aproximately 450 ns and on falling edge aproximately 451 ns. For 3.3 V supply voltage is the response time 314 ns on rising edge and 316 ns on falling edge.

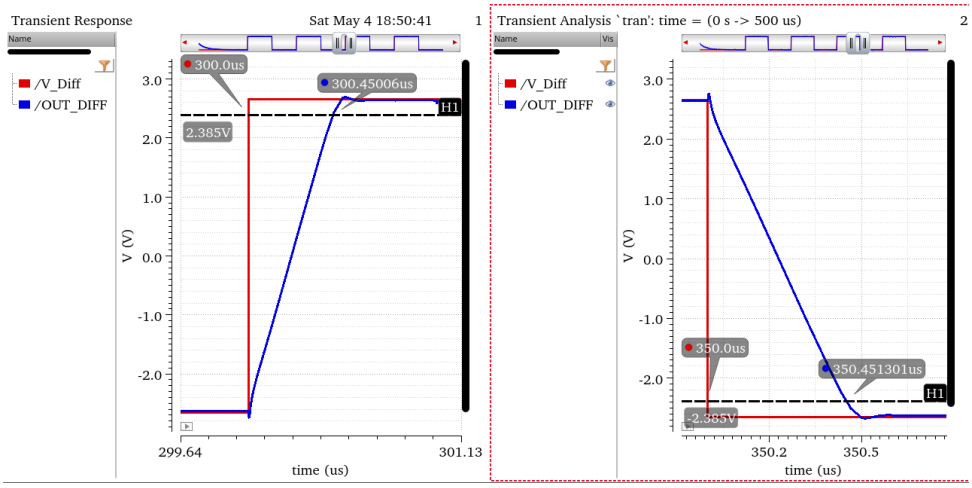

Figure 7.5: Response time of the equalizer circuit with supply voltage of 5 V

7.3 Equalizer frequency behavior and compensation evaluation

Now that it is assured that the circuit is stable in all implementations and under all circumstances, and given that both offset and power consumption are well below the maximal limits, the compensating capabilities of the circuit can be verified.

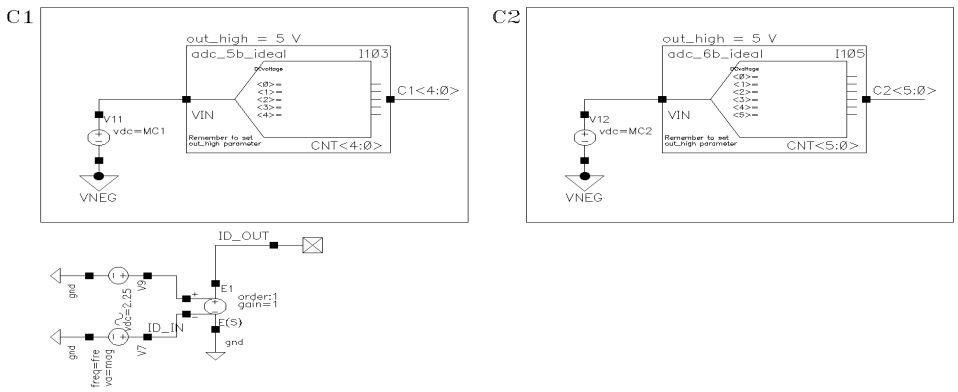

Figure 7.6: Sources used to configure capacitor matrixes C_1 and C_2 and ideal frequency responses

To evaluate the circuit's frequency responses, reference is needed; therefore, the sources shown in Figure 7.6 are used. The ideal ADC converters are blocks used to select a desired number of elementary capacitors connected to the circuit. The number of each is set up as a voltage written to the parameters of the DC sources V11 and V12. Source E1 from the figure serves as an ideal source, with its parameters being poles and zeros. These poles and zeros are calculated from the number of elementary capacitors used. Source

E1 realizes the best-chosen approximations found in Matlab while designing the capacitor matrixes.

Frequency responses generated by source E1 will be referred to as ideal frequency responses in subsequent text, and they serve as basis to evaluate the frequency behavior of the equalizer circuit. However, it is important to note that the error between the equalizer frequency response and the ideal function generated by source E1 must be evaluated, considering the error originating from the approximation to the results of the notch frequency behavior. Thus, there are two sources of errors which can either compound or cancel each other out.

The frequency response of the equalizer circuit is obtained as a result of the periodic AC analysis, which must be used because the circuit is switched. To obtain representative results out of these simulations, the magnitude frequency responses of the ideal source and differential output of the equalizer are divided. This division yields the error function. The maximal error on the interval up to 3 kHz is then determined from this error function. Similarly, the phase frequency response is evaluated. Thresholds for maximal errors are established to facilitate the evaluation of results and to eliminate the need for exporting all waveforms and comparing them in Matlab with notch simulations. The threshold of maximal error on intervals up to 3 kHz are set to 0.85 % in magnitude and 0.5° in phase. These thresholds are approximate values that ensure compensation requirements should be met if all results fall below these values.

As in the case of stability simulations, the initial step was to run nominal simulations for all unique configurations. These simulations attest to the circuit's ability to compensate for various frequency responses. The maximal errors obtained from the simulations indicate, that the most problematic frequency responses to compensate are those with the highest gains and phase shifts. These typically correspond to notches with large dimensions and small air gaps, as they exhibit the greatest attenuations.

The next step in verification involved subjecting the worst-performing circuit configurations to a Worst-case Monte Carlo simulation to determine whether they meet the thresholds or even requirements. The summary of the Worst-case Monte Carlo results for the most problematic combination (MC1 = 20, MC2 = 21) is presented in Table 7.3.

Parameter	**Min.**	**Max.**	**Mean**	**Threshold**
Mag. Error 3 kHz	0.024 %	0.820 %	0.262 %	0.8 %
Phase Error 3 kHz	0.061°	0.594°	0.198°	0.5°
Mag. Error 20 kHz	0.394 %	2.391 %	0.940 %	4 %

Table 7.3: Worst-case Monte Carlo results summary

As can be seen in Table 7.3, the worst phase results are above the threshold of 0.5°, but still well under the requirement of 1°. This outcome is not optimal, because the margin for error between the ideal frequency response and the simulated initial notch frequency response is smaller than expected. The

maximal magnitude error originates from Monte Carlo run with t = -40 °C and supply voltage 5.5 V, while the maximal error in phase arises from the run with t = 170 °C and supply voltage 4.5 V. Complete results indicate that with higher temperatures, the magnitude errors decrease, but phase errors increase overall. Complete results are stated in Appendix A in Figure A.1 and A.2.

In Figure 7.7, the results of maximal magnitude and phase errors for frequencies up to 3 kHz from the Monte Carlo simulation run under nominal conditions are illustrated. The results of magnitude error are on the top of the figure and phase error results are on the bottom. In this run, all resulting errors are within the specified thresholds, which are visualised by the line between green and red backroud.

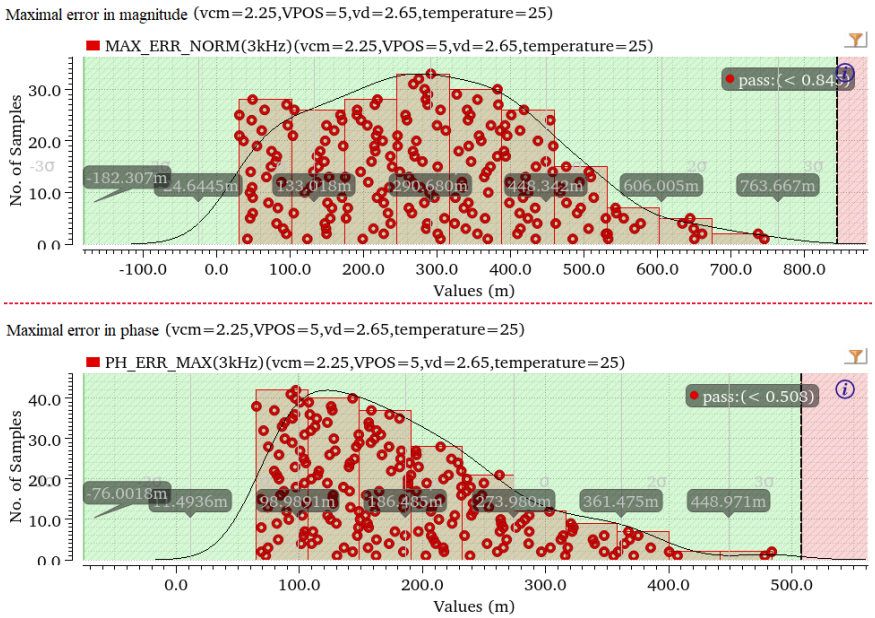

Figure 7.7: Nominal conditions Monte Carlo results of maximal magnitude and phase errors up to 3 kHz

In addition to the worst-performing equalizer configurations, a representative sample of other configurations was also subjected to Worst-case Monte Carlo simulations. This sample included combinations with both low-pass and high-pass frequency characteristics and with various gains.

These Worst-case Monte Carlo simulations revealed two key findings. The first rather convenient result is that across all tested circuit configurations, the same seven Monte Carlo corners consistently exhibit the worst performance in both magnitude and phase. This simplifies further simulations, as all used configurations can be tested in these corners to identify the worst-case scenarios, avoiding the extreme time consumption that would be required to run Worst-case Monte Carlo simulations for every configuration.

Conversely, the second finding is more concerning. It was observed that when the filter's gain is relatively low, the pole and zero positions are close to

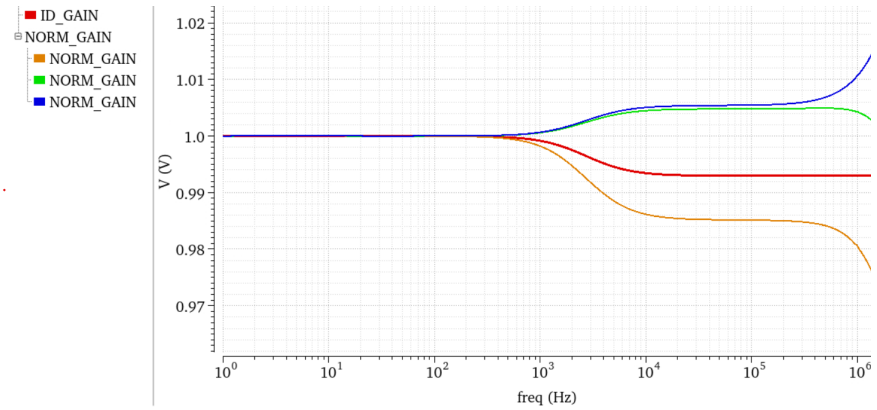

Figure 7.8: Change of equalizer frequency response in worst-case Monte Carlo corners (MC1 = 22, MC2 = 62)

each other. In the worst Monte Carlo corners, because of process imperfections and temperature, the position of the pole and zero can interchange. This alters the frequency response of equalizer from low pass to high pass leading to larger errors while still remaining under given thresholds. This finding is troubling, because in these cases the equalizer circuit enhances the notch frequency behavior, which may lead to larger final errors than in other cases. The waveforms illustrating this finding are in Figure 7.8. The red waveform in the middle is ideal, orange one illustrates expected waveform due to extreme conditions. Blue and green waveforms are examples of problematic Monte Carlo corners in which the characteristics is changed from low pass to high pass.

With the identification of the worst-performing Monte Carlo corners, all 639 utilized circuit configurations can be simulated within these corners under all temperatures and voltages from Table 6.1 to obtain the worst-case scenarios for all configurations and verify whether the designed equalizer meets the compensation requirements.

7.3.1 Worst-case scenarios results

Simulating all equalizer configurations in the worst-case corners confirmed the initial finding that the largest errors occur in configurations with the highest gains. These worst-case corners of the most error-prone equalizer circuit configurations are to be exported from Cadance to verify the resulting characteristics against the initial notch simulations. Similarly, configurations in which equalizer changes its frequency characteristic from low-pass to high-pass, and vice versa, are also to be exported for verification.

As previously stated, while designing the capacitor matrixes, the best compensating frequency response was identified for each simulated notch dimension and air gap size. However, this discretization introduced compensation errors. To identify the overall worst-case scenarios and verify them, the worst cases in circuit implementation and worst cases in finding compensating frequency responses must be determined.

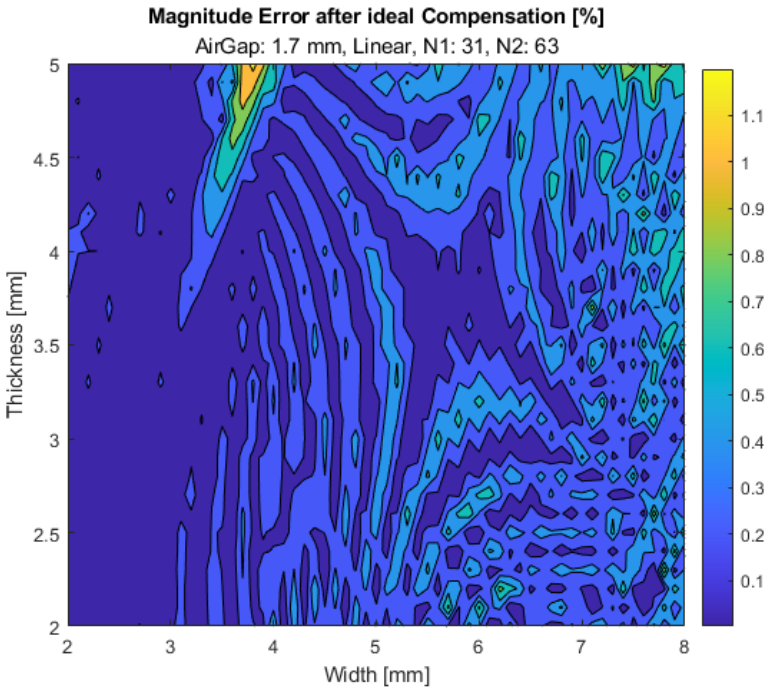

Figure 7.9: Maximal magnitude error after ideal compensation up to 3 kHz

Figure 7.9 illustrates the error in magnitude for all notch frequency responses with an air gap of 1.7 mm on frequencies up to 3 kHz caused by the discrete number of realizable compensating frequency responses of the equalizer. Figure 7.10 presents the corresponding phase shift errors. As shown in these figures, the error is negligible in most cases; however, some errors approach half of the requirements.

If any case across all notch and air gap sizes exhibits an error after compensation by ideal discrete compensation bigger than 0.8 % in magnitude or 0.4° in phase, its corresponding equalizer configuration is also submitted for verification with initial notch simulations. Figures 7.9 and 7.10 demonstrate that even at the low air gap level, the number of such cases is relatively low, and most are located in the area of large notch width.

These criteria resulted in 49 unique equalizer configurations for which the worst-case corners were exported and verified against initial simulations of notch frequency characteristics. Verification was performed as follows: the magnitude frequency response of all worst-case corners for each of the 49 configurations was successively multiplied by all notch magnitude frequency responses that it compensated and the final error functions for each of these notch frequency responses were ploted. The same procedure was applied to phase frequency responses, but with summation instead of multiplication. If all points up to 3 kHz of these error functions are under the requirements thresholds of 2 % in magnitude and 1° in phase the equalizer compensation satisfies the requirements.

Figure 7.11 displays a graph of error waveforms of the equalizer configura-

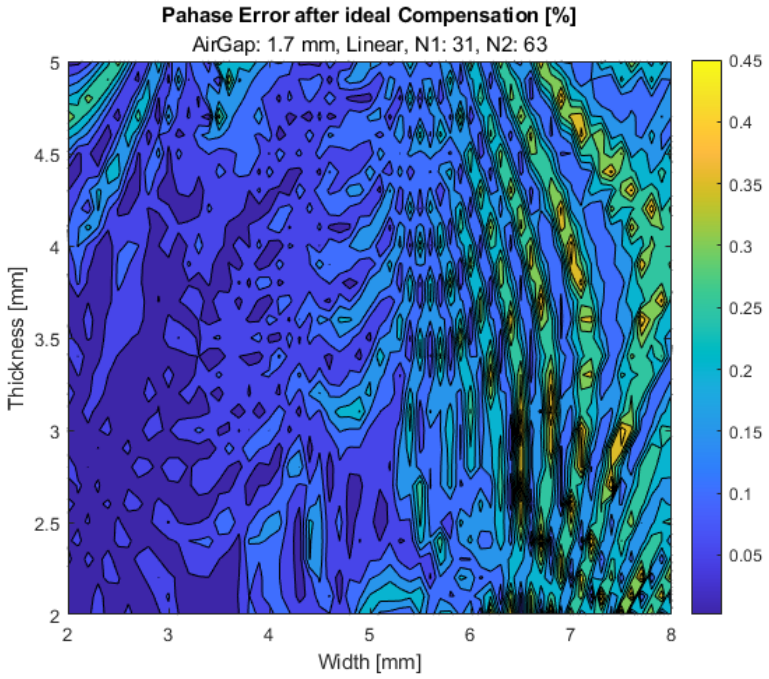

Figure 7.10: Maximal phase error after ideal compensation up to 3 kHz

tion that, after final evaluation, was deemed the worst in magnitude. The configuration is MC1 = 27 and MC2 = 42, and the maximal magnitude error on intervals up to 3 kHz is 1.947 %, which is less than the 2 % requirement. Therefore, the first magnitude compensation requirement is met.

Figure 7.12 depicts graph of error waveforms of the equalizer configuration which after final evaluation ended up being the worst out of all in phase compensation. The configuration is MC1 = 18 and MC2 = 24, and the maximal phase error on intervals up to 3 kHz is -0.986° which is also less than the 1° requirement. Therefore, the phase compensation requirement is met.

The final compensation requirement is to compensate the magnitude on interval up to 20 kHz with precision of 10 %. This requirement was marginalized throughout the design and evaluation process as it was much less critical than the two previous ones. Figure 7.13 shows graph of error waveforms of the equalizer configuration that performed the worst after final evaluation. The configuration is MC1 = 29 and MC2 = 38, and the total magnitude error on intervals up to 20 kHz is -5.623 % which is much less than the 10 % requirement. Therefore, the second magnitude compensation requirement is met as well.

In conclusion, all specified requirements were met, confirming the successful design of the equalizer. Furthermore, most of these worst-case scenarios occur for exotic notch dimensions, which may never even be utilized. For instance, the worst phase error corresponds to a notch with dimensions 7.5x2 mm and airgap 1.7 mm, while the worst magnitude error up to 3 kHz is associated with a notch measuring 7.4x4.7 mm and an air gap of 1.8 mm.

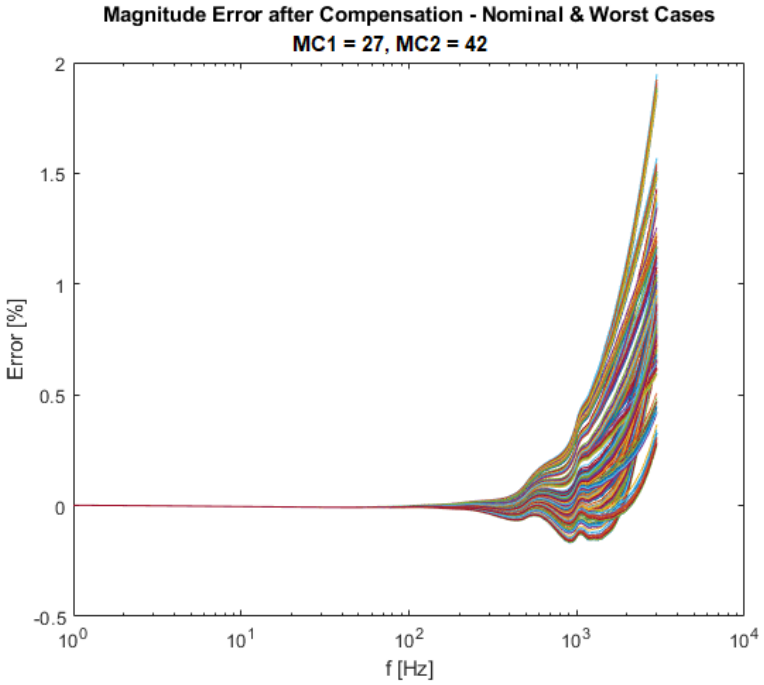

Figure 7.11: Final worst-case magintude compensation error functions up to 3 kHz

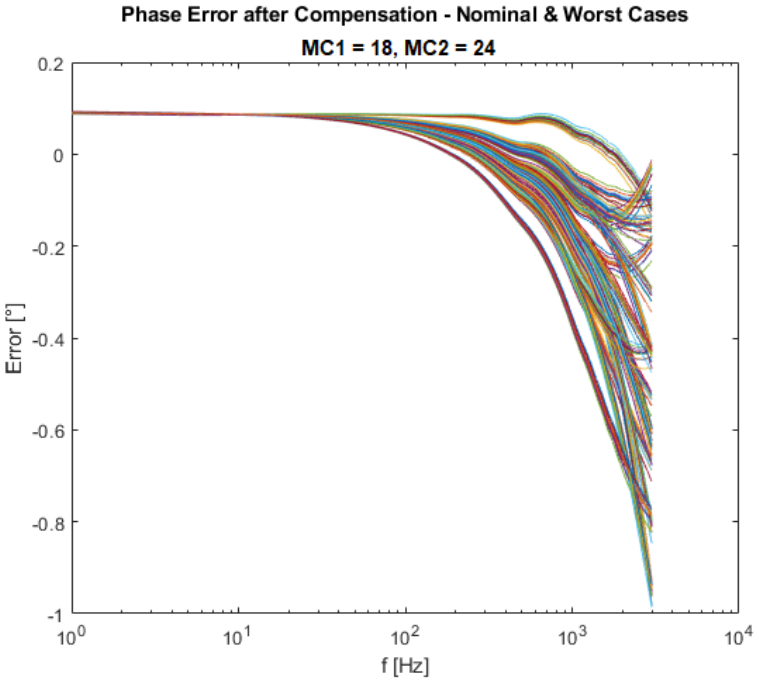

Figure 7.12: Final worst-case phase compensation error functions up to 3 kHz

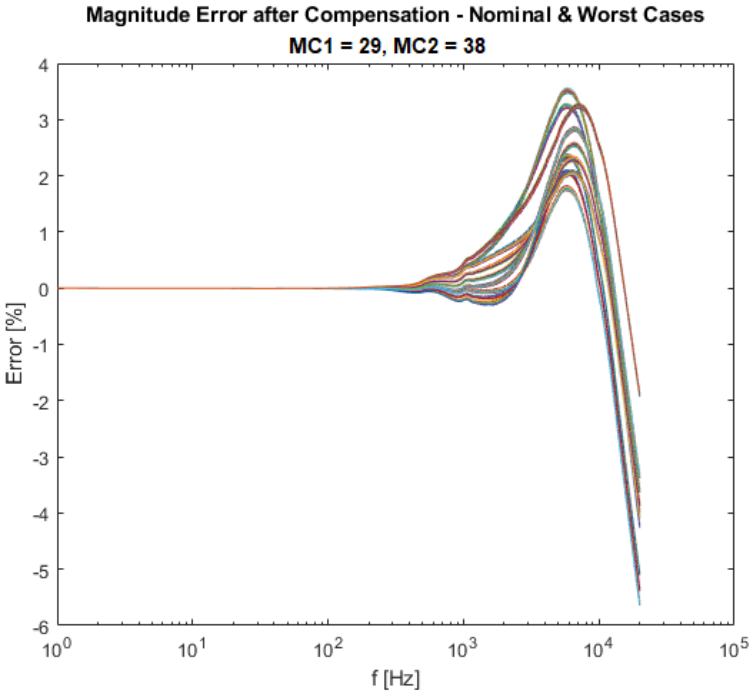

Figure 7.13: Final worst-case magnitude compensation error functions up to 20 kHz

7.3.2 Compensation of typical application

The previous section identified the worst-case scenarios to determine if the circuit meets all requirements in all of the scenarios, which it does. This chapter aims to demonstrate the effectiveness of the compensation in a typical application. For this purpouse, a notch with dimensions 5x4 mm and a 2.5 mm air gap was selected, as it falls within the typical dimensions listed in Table 3.1. Figure 7.14 shows the frequency characteristics of the notch, showing a maximal attenuation of -4.388 % and a phase shift of -4.227° for frequency intervals up to 3 kHz.

After applying the ideal compensation determined in Matlab simulations, the maximal error from constant level on given frequency interval is 0.242 % in magnitude and 0.162° in phase. The equalizer configuration of capacitor matrixes used to compensate for this notch frequency characteristics is MC1 = 13 and MC2 = 31.

This equalizer configuration was simulated under nominal conditions and worst-case Monte Carlo corners. The resulting frequency responses of the equalizer were exported to Matlab and compared against initial simulation of the notch frequency response.

The final magnitude compensation error results are presented in Figure 7.15. The worst compensation of gain nominal conditions is -0.151 %. Compensation of worst-case Monte Carlo corners results in even better compensation, with the worst error being 0.137 %. All these results surpass the compensation achieved by the ideal frequency response.

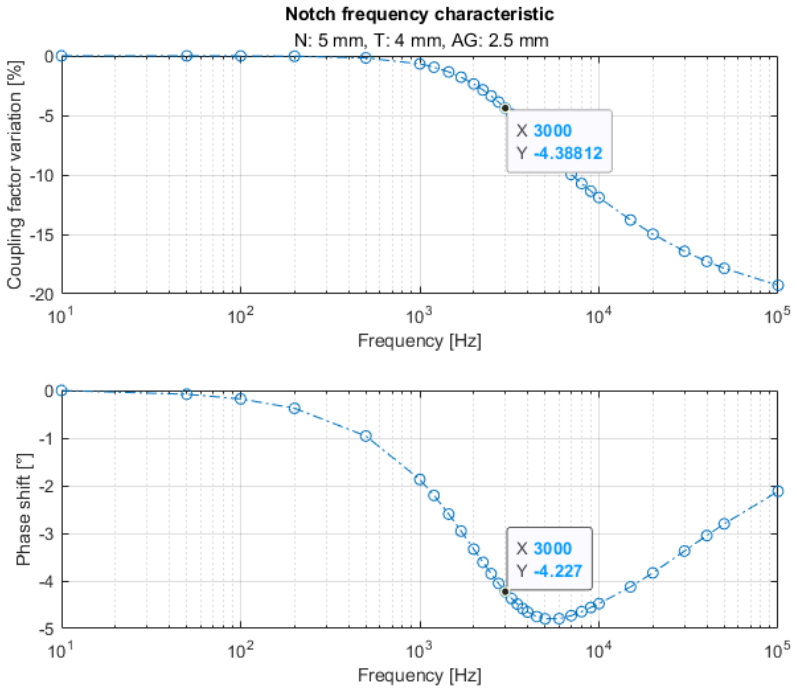

Figure 7.14: Typical notch frequency characteristic ($N = 5$ mm, $T = 4$ mm, $AG = 2.5$ mm)

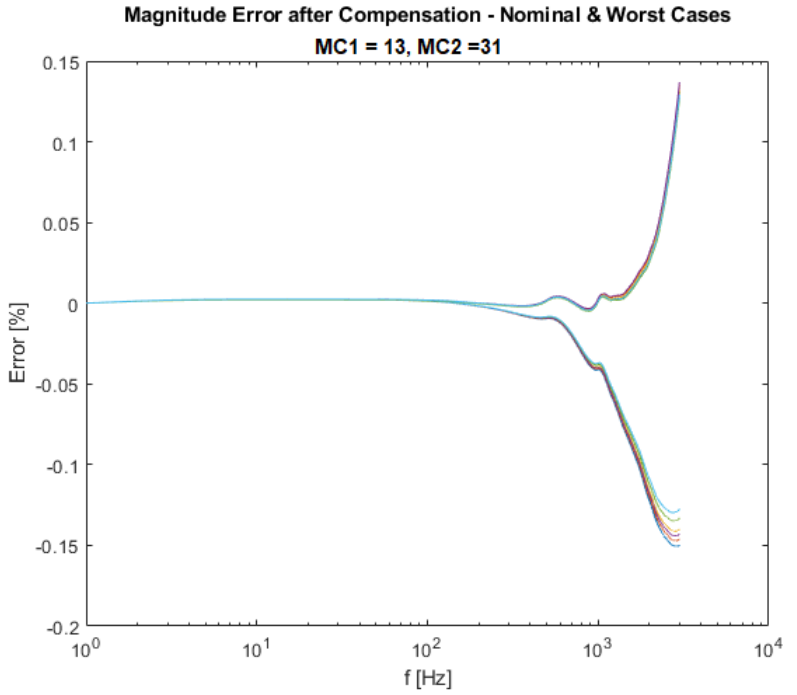

Figure 7.15: Final magnitude compensation error functions of typical application up to 3 kHz

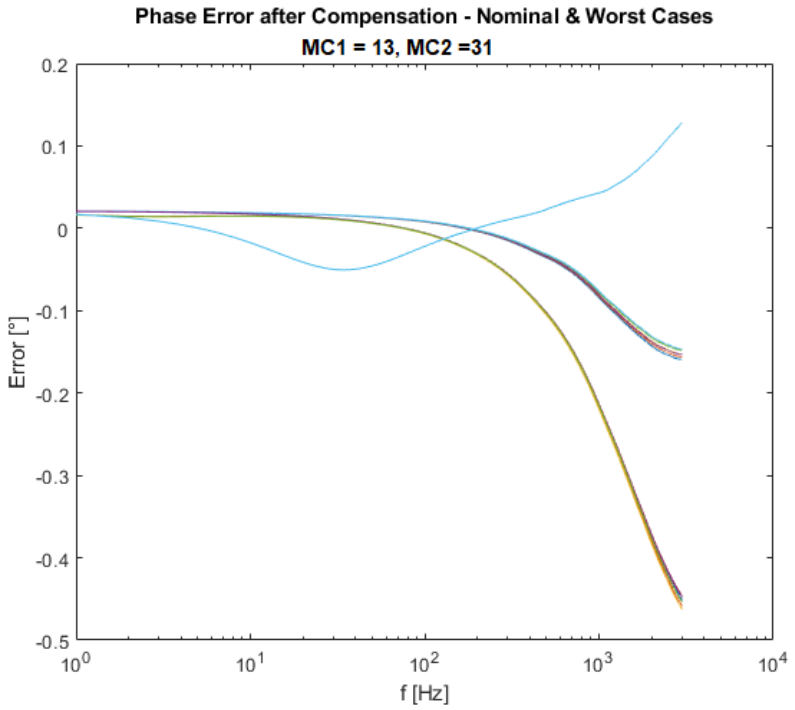

Figure 7.16: Final phase compensation error functions of typical application up to 3 kHz

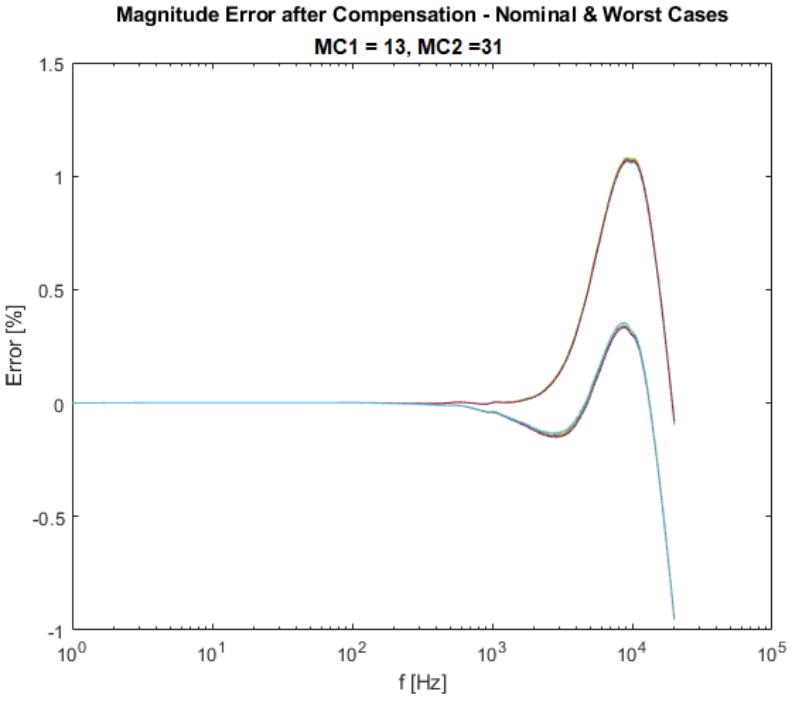

Figure 7.17: Final magnitude compensation error functions of typical application up to 20 kHz

Phase shift compensation errors are shown in Figure 7.16. The worst error for nominal conditions is -0.159°. Unlike magnitude compensation, the phase compensation in the worst-case Monte Carlo corners is worse than under nominal conditions, with the worst error being -0.463°.

Lastly, the magnitude compensation error for intervals up to 20 kHz has the worst error of 1.081 %, which is significant improvement compared to the uncompensated attenuation of -15 % at 20 kHz. These results are illustrated in Figure 7.17.

When comparing the results obtained by the final evaluation to the initial attenuations, it is evident that the equalizer significantly improves performance, successfully compensating for both attenuation and phase shift across frequencies.

Chapter 8

Layout

The final chapter of this thesis is dedicated to the layout design of the equalizer, which represents the concluding step in creating the block for the integrated circuit.

8.1 Capacitor matrixes cells layout

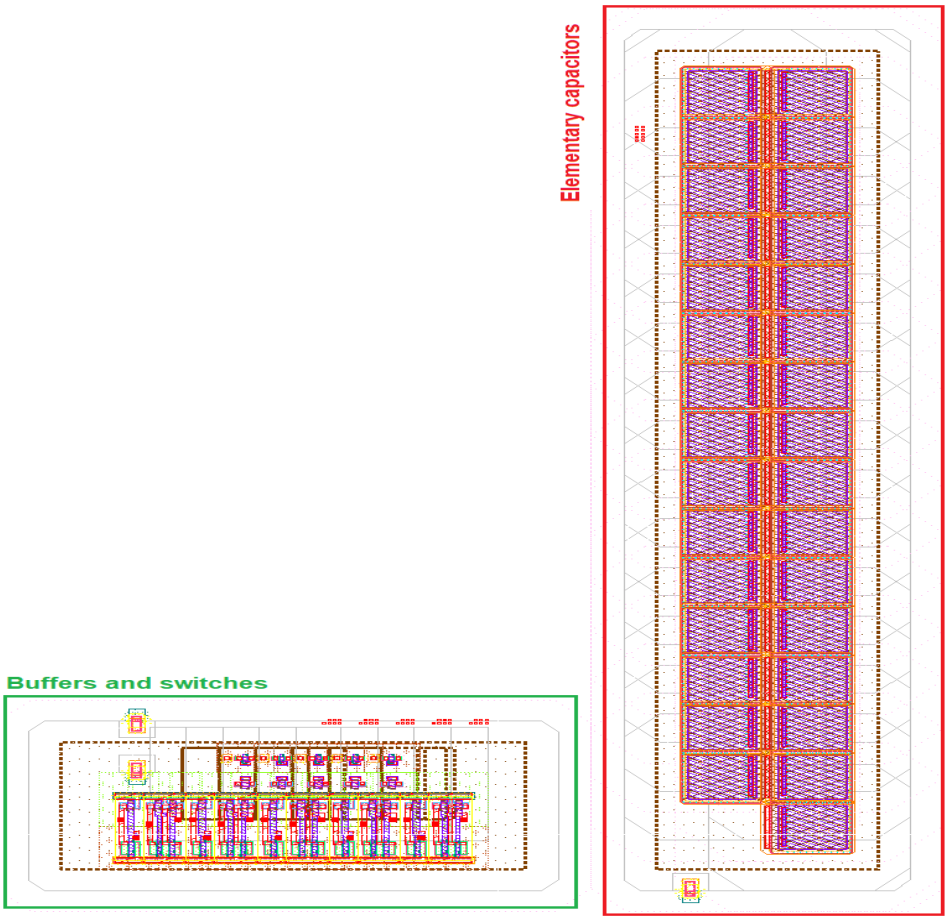

Figure 8.1: Layout of the C_1 capacitor matrix cell

Similarly, as in the case of designing the circuit also the layout starts from the individual cells of the whole circuit. The layout of the first cell, the C_1 capacitor matrix cell, is presented in Figure 8.1. On the right side of the figure oriented vertically, are the elementary capacitors. The smaller horizontal rectangle consists of transmission gates, responsible for connecting the capacitors to the circuit, along with buffers for the control signal of the transmission gates.

The two parts of this cell may appear unnecessarily distant. This separation is required because each part must reside in its own N-well pocket, with these pockets connected to different potentials.

The second layout is presented in Figure 8.2, it is layout of C_1 capacitor matrix cell. Here, the elementary capacitors are positioned at the top while transmission gates and buffers are at the bottom of the figure.

The areas of the cells are following:

- **C_1:** 9 650 µm^2
- **C_2:** 6 700 µm^2

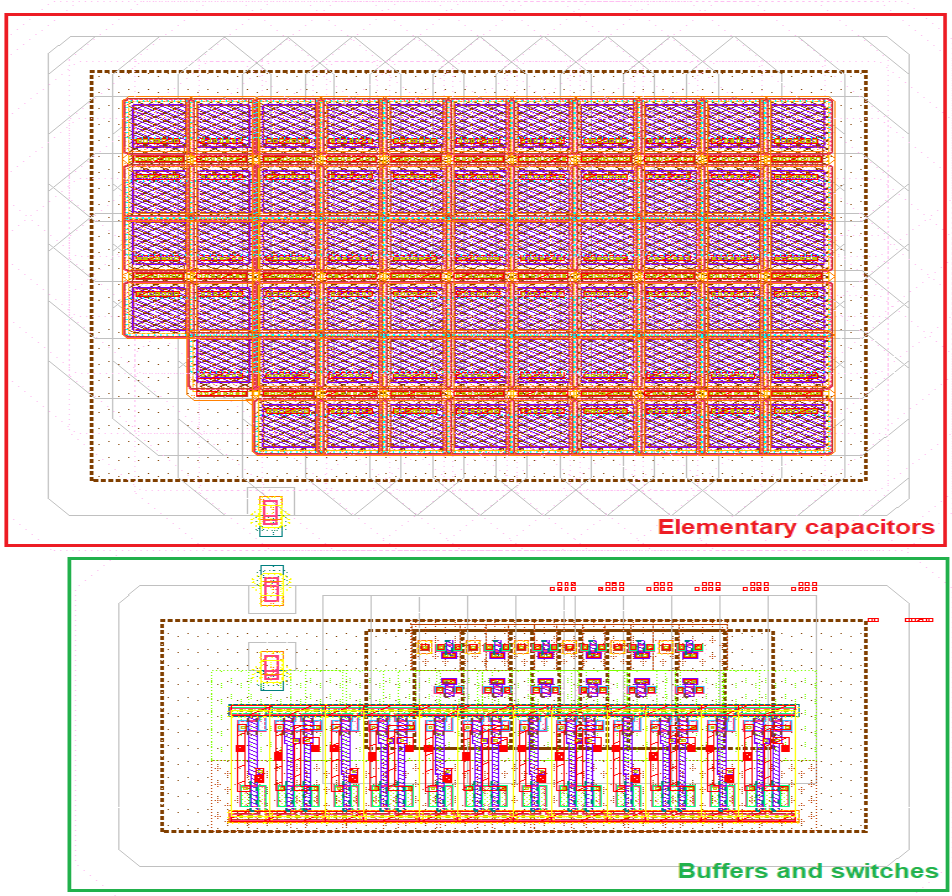

Figure 8.2: Layout of the C_2 capacitor matrix cell

8.2 Fully differential operational amplifier layout

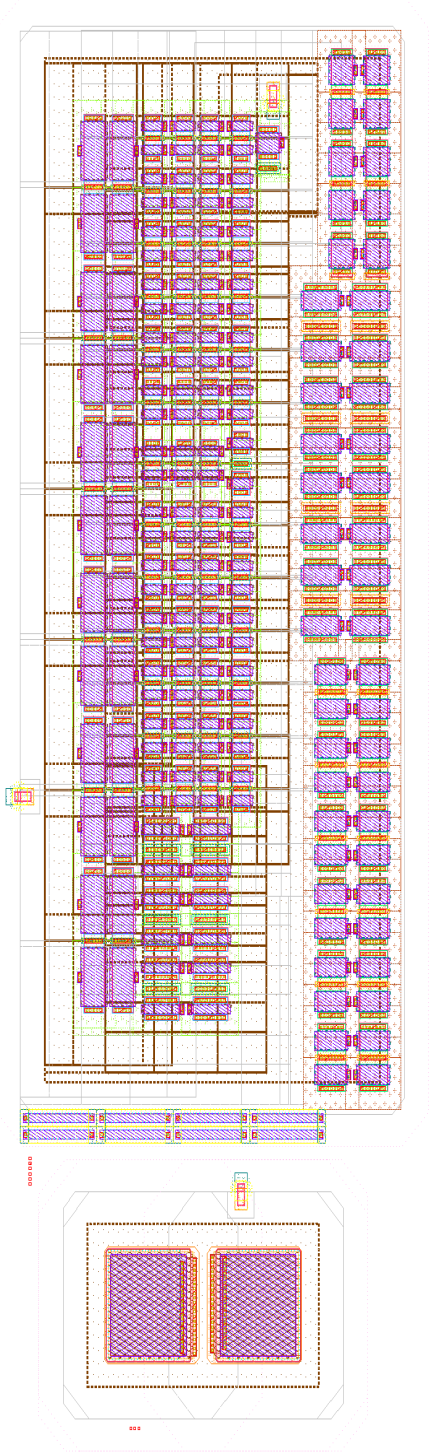

Figure 8.3: Layout of the fully differential operational amplifier

Figure 8.3 depicts the layout of the designed fully differential operational amplifier. The arrangement of the individual components is similar to the schematic. The longer transistors on the left side of the Figure 8.3 are NMOS transistors responsible for current management. The multitude of small transistors in the center are the output transistors and the first stage's common-mode feedback transistors. Below the output transistor is a differential pair from the common-mode circuit. From top to bottom on the right side, the figure shows the current mirror supplying tail current to the input stage, the transistors of the input differential pair, the active load of the output stage and the common-mode feedback circuit. At the bottom of the Figure 8.3 resistor form common-mode feedback circuit and compensating capacitors are situated.

The area of the layout is:

- 9 280 μm^2

8.3 Equalizer layout

The final layout of the entire equalizer, which is assembled from the layout blocks of the cells, is depicted in Figure 8.4. As can be seen the operational amplifier is placed in the middle with the switched capacitors and its switches and it is surrounded by capacitor matrixes cells.

Each individual block resides in its own N-well pocket, which need certain spacing to others. While this may seem to be a waste of space, it allows for flexibility in repairs. If an issue arises with this block or other parts of the integrated circuit, adjustments can be made solely to the metal layers if each block has its own N-well pocket. Otherwise, all lithography masks would have to be recreated, incurring significant costs. Therefore, this trade-off of space for repair flexibility is deemed acceptable.

The total area of the whole equalizer layout is:

- 44 860 μm^2

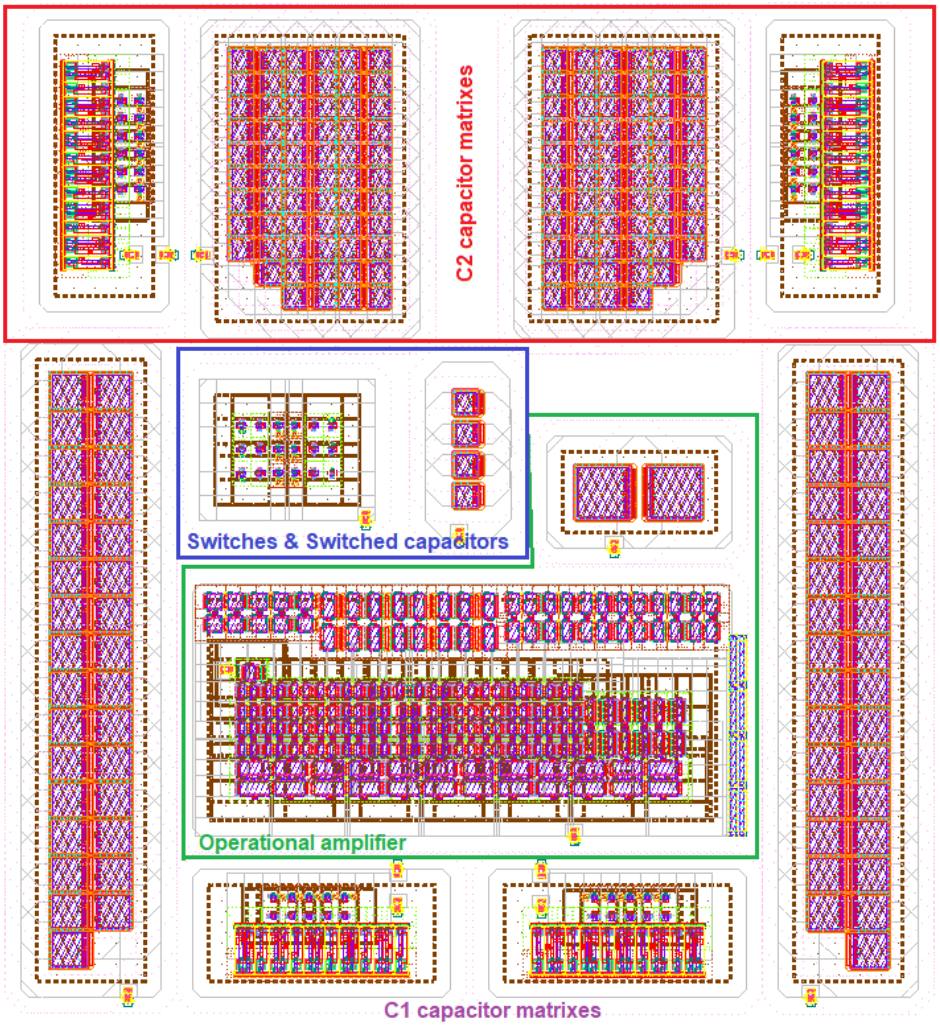

Figure 8.4: Layout of the complete equalizer circuit

Chapter 9

Conclusion

The main goal of this research was to design an analog equalizer for the coreless Hall-effect current sensor ACS37610. This endeavor was driven by the demand for improvements in coreless current sensing, propelled by the growth of the automotive industry - particularly in electric vehicles - and the escalating safety standards in related sectors. This type of Hall-effect sensor is used to measure large currents in the notches of busbars, where eddy currents generated at higher frequencies decrease the accuracy of the measurement. The equalizer designed in this thesis compensates for this phenomenon across a wide spectrum of notch sizes and distances between the notch and sensor.

To achieve the objective of designing the equalizer, the behavior of the notch over frequency had to be inspected. When the sensor was located on the longer side of the notch, the frequency response behaved as a low-pass filter, whereas with the sensor positioned above the shorter side of the notch, its frequency response behaved like a high-pass filter. Also, the closer the proximity of the sensor to the notch, the more significant the attenuations or amplifications were. It was found that the notch frequency responses can be described using first-order transfer functions with one left-plane real pole and one left-plane real zero. With the form of the transfer function describing the notch's frequency response, the form of the compensating transfer functions was determined.

Once the transfer function of the compensation was known, the appropriate circuit implementation could be selected. Out of four considered implementations, the one using a fully differential operational amplifier with capacitor matrixes - used to adjust the filter to the required compensating frequency response - and resistors realized by switched capacitors due to their large value was selected.

There are two capacitor matrixes consisting of elementary capacitors, and by connecting them into the circuit, frequency responses able to compensate for all possible notch frequency responses are obtained. The number of elementary capacitors in each matrix had to be determined with the desire for the lowest number possible. The number of elementary capacitors was determined to be 31 and 63.

To complete the circuit design, a fully differential operational amplifier was designed and tested within a temperature range of -40 °C to 170 °C and

supply voltage ranges from 3 V to 3.6 V and from 4.5 V to 5.5 V. The Monte Carlo simulations across these parameter ranges provided satisfying results. The worst-case phase margin was 57.28°, which is well above the lower limit of 45°. The DC open-loop gain lower limit was 70 dB, and the worst-case for the designed operational amplifier was 74.35 dB. Parameters like offset and bandwidth were also met in all conditions. The power consumption was far below the maximum allowed value of 415 µA, with the worst-case scenario showing consumption of only 185.6 µA.

With the verified operational amplifier, the entire equalizer circuit was assembled and verified. In the initial design, the switches of the switched capacitors were realized using NMOS transistors; however, they were insufficient for larger input voltages and clamped signals. Therefore, where needed, they were replaced by transmission gates, and the total number of switches was reduced as some of them were redundant.

After these adjustments, the equalizer's circuit stability was again verified, as the feedback loop connection has a significant impact on the stability of the circuit. The stability of the circuit was verified across the mentioned temperature and voltage ranges. Moreover, the equalizer circuit can be configured in many distinct ways. For all the configurations used for compensation of the notch frequency behavior, the worst-case scenarios were simulated. None of the cases for any of the circuit configurations had a phase margin below 45°, with the worst being 45.79°. The offset and power consumption remained almost the same as in the case of simulating the operational amplifier alone.

The worst-case frequency responses were verified against the notch's initial simulations of its frequency responses. All three requirements were met in all cases over the temperature and voltage ranges. The error after magnitude compensation must be smaller than 2 % up to 3 kHz. The worst scenario was 1.947 %. The magnitude compensation up to 20 kHz must be better than 10 %. The worst-case scenario was -5.623 %. For phase compensation up to 3 kHz, the worst-case scenario was -0.986°, with the maximum allowed value being 1°.

To complete the whole block, layout of the equalizer was done, with total area of 44,860 µm².

The main oblectives of this thesis, compensation error in magnitude less than 2 % and in phase less than 1° up to 3 kHz and compensation error in magnitude less than 10 % up to 20 kHz, were successfully fulfilled with worst results being 1.947 %, -0.986°, 5.623 % respectively.

In the future this circuit can be modified by changing values of elementary capacitors to be implemented to other coreless sensors such as ACS37612. The improvement considered for future work is to design more sophisticated architecture of switched capacitors to average input signals.

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Appendix A

Complete Monte Carlo results

Test	Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
Overall Yield Estimate: 98.5 %(197 passed/200 pts) Confidence Level: <not set> Filter: <not set>									
Yield Estimate: 99.5 %(199 passed/200 pts) | Parameters: vcm=1.5,VPOS=3,vd=1.75,temperature=-40									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	75.47 °	> 45	85.26 °	82.3 °	1.556 °	7.99	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	23.5 m%	< 0.845	649.6 m%	217.8 m%	135.5 m%	1.54	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	399.7 m%	< 10	1.985 %	945.2 m%	340.2 m%	8.87	0
	PH_ERR_MAX(3kHz)(summary)	99.5% (199/200)	63.79 m°	< 0.508	509.7 m°	206.6 m°	95.47 m°	1.05	0
	DIFF_OFF(summary)	100% (200/200)	-5.894m	range -12.6m 12.6m	5.442m	25.34u	2.259m	1.86	0
	I_ALL(summary)	100% (200/200)	81.03 uA	< 415	158.5 uA	125.7 uA	13.65 uA	1.01e+7	0
Yield Estimate: 99 %(198 passed/200 pts) | Parameters: vcm=1.5,VPOS=3,vd=1.75,temperature=25									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	77.85 °	> 45	85.56 °	82.83 °	1.273 °	9.91	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	26.46 m%	< 0.845	658.6 m%	224.4 m%	138.2 m%	1.5	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	405.7 m%	< 10	1.973 %	935.8 m%	337.5 m%	8.95	0
	PH_ERR_MAX(3kHz)(summary)	99% (198/200)	61.67 m°	< 0.508	520.2 m°	214.7 m°	96.85 m°	1.01	0
	DIFF_OFF(summary)	100% (200/200)	-5.846m	range -12.6m 12.6m	5.416m	24.56u	2.239m	1.87	0
	I_ALL(summary)	100% (200/200)	91.08 uA	< 415	156.1 uA	129.3 uA	11.58 uA	1.19e+7	0
Yield Estimate: 99 %(198 passed/200 pts) | Parameters: vcm=1.5,VPOS=3,vd=1.75,temperature=170									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	80 °	> 45	86.37 °	84.05 °	972.6 m°	13.4	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	34.6 m%	< 0.845	576.1 m%	203.7 m%	117.3 m%	1.82	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	397.7 m%	< 10	1.98 %	937.5 m%	342.4 m%	8.82	0
	PH_ERR_MAX(3kHz)(summary)	99% (198/200)	67.61 m°	< 0.508	538.1 m°	221.1 m°	99.17 m°	0.964	0
	DIFF_OFF(summary)	100% (200/200)	-5.721m	range -12.6m 12.6m	5.343m	22.6u	2.188m	1.92	0
	I_ALL(summary)	100% (200/200)	106.5 uA	< 415	156.3 uA	136.4 uA	9.039 uA	1.53e+7	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=1.5,VPOS=3.3,vd=1.75,temperature=-40									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	74.61 °	> 45	84.3 °	81.32 °	1.444 °	8.39	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	27.07 m%	< 0.845	684.6 m%	239.5 m%	143.4 m%	1.41	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	425.8 m%	< 10	1.972 %	940.9 m%	335.4 m%	9	0
	PH_ERR_MAX(3kHz)(summary)	100% (200/200)	67.76 m°	< 0.508	493.3 m°	194.8 m°	91.71 m°	1.14	0
	DIFF_OFF(summary)	100% (200/200)	-5.874m	range -12.6m 12.6m	5.43m	25.06u	2.251m	1.86	0
	I_ALL(summary)	100% (200/200)	85.17 uA	< 415	163 uA	130.4 uA	13.75 uA	1.01e+7	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=1.5,VPOS=3.3,vd=1.75,temperature=25									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	77.23 °	> 45	84.72 °	82.26 °	1.194 °	10.4	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	28.24 m%	< 0.845	686.7 m%	241.6 m%	144.1 m%	1.4	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	429.3 m%	< 10	1.962 %	932.9 m%	333.5 m%	9.06	0
	PH_ERR_MAX(3kHz)(summary)	100% (200/200)	65.43 m°	< 0.508	504 m°	203 m°	93.74 m°	1.08	0
	DIFF_OFF(summary)	100% (200/200)	-5.831m	range -12.6m 12.6m	5.407m	24.34u	2.233m	1.88	0
	I_ALL(summary)	100% (200/200)	94.59 uA	< 415	159.8 uA	133.2 uA	11.65 uA	1.19e+7	0
Yield Estimate: 99.5 %(199 passed/200 pts) | Parameters: vcm=1.5,VPOS=3.3,vd=1.75,temperature=170									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	80.87 °	> 45	85.94 °	84.07 °	890.4 m°	14.6	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	35.76 m%	< 0.845	585.2 m%	212.5 m%	115 m%	1.83	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	394 m%	< 10	1.967 %	934.6 m%	340.9 m%	8.86	0
	PH_ERR_MAX(3kHz)(summary)	99.5% (199/200)	68.17 m°	< 0.508	520.6 m°	206.5 m°	94.79 m°	1.06	0
	DIFF_OFF(summary)	100% (200/200)	-5.714m	range -12.6m 12.6m	5.337m	22.51u	2.186m	1.92	0
	I_ALL(summary)	100% (200/200)	109.1 uA	< 415	159 uA	139.3 uA	9.078 uA	1.52e+7	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=1.5,VPOS=3.6,vd=1.75,temperature=-40									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	73.86 °	> 45	83.01 °	80.02 °	1.37 °	8.52	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	24.94 m%	< 0.845	731.6 m%	274.4 m%	154.1 m%	1.23	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	445.6 m%	< 10	1.953 %	934 m%	326.7 m%	9.25	0
	PH_ERR_MAX(3kHz)(summary)	100% (200/200)	63.5 m°	< 0.508	481 m°	184.6 m°	87.51 m°	1.23	0
	DIFF_OFF(summary)	100% (200/200)	-5.859m	range -12.6m 12.6m	5.42m	24.86u	2.245m	1.87	0
	I_ALL(summary)	100% (200/200)	88.37 uA	< 415	166.6 uA	133.9 uA	13.83 uA	1e+7	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=1.5,VPOS=3.6,vd=1.75,temperature=25									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	76.4 °	> 45	83.76 °	81.1 °	1.171 °	10.3	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	29.6 m%	< 0.845	720.9 m%	268.9 m%	152.1 m%	1.26	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	439 m%	< 10	1.944 %	926.6 m%	326.4 m%	9.27	0
	PH_ERR_MAX(3kHz)(summary)	100% (200/200)	66.44 m°	< 0.508	491.7 m°	193.2 m°	90.2 m°	1.16	0
	DIFF_OFF(summary)	100% (200/200)	-5.82m	range -12.6m 12.6m	5.4m	24.2u	2.229m	1.88	0
	I_ALL(summary)	100% (200/200)	97.37 uA	< 415	162.8 uA	136.2 uA	11.71 uA	1.18e+7	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=1.5,VPOS=3.6,vd=1.75,temperature=170									
CS_IP_Equalizers_Diff_Mill_swc_1									
	PhaseMargin_Diff(summary)	100% (200/200)	80.2 °	> 45	85.46 °	83.34 °	941.3 m°	13.6	0
	MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	38.58 m%	< 0.845	587.9 m%	226.3 m%	116.2 m%	1.78	0
	MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	404.6 m%	< 10	1.966 %	930.9 m%	338.1 m%	8.94	0
	PH_ERR_MAX(3kHz)(summary)	100% (200/200)	65.28 m°	< 0.508	493.4 m°	195.6 m°	90.82 m°	1.15	0
	DIFF_OFF(summary)	100% (200/200)	-5.708m	range -12.6m 12.6m	5.334m	22.48u	2.184m	1.92	0
	I_ALL(summary)	100% (200/200)	111.2 uA	< 415	161.3 uA	141.5 uA	9.112 uA	1.52e+7	0

Figure A.1: Complete results of Monte Carlo simulations 3.3 V device

Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=2.25,VPOS=4.5,vd=2.65,temperature=-40								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	74.97 °	> 45	83.19 °	80.37 °	1.234 °	9.55	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	26.22 m%	< 0.845	704.6 m%	253.3 m%	147.9 m%	1.33	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	441.8 m%	< 10	1.985 %	944.5 m%	334.1 m%	9.03	0
PH_ERR_MAX(3kHz)(summary)	100% (200/200)	61.44 m°	< 0.508	486.1 m°	188.9 m°	89.84 m°	1.18	0
DIFF_OFF(summary)	100% (200/200)	-5.851m	range -12.6m 12.6m	5.415m	24.74u	2.241m	1.87	0
I_ALL(summary)	100% (200/200)	95.39 uA	< 415	176.8 uA	142.8 uA	14.34 uA	9.65e+6	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=2.25,VPOS=4.5,vd=2.65,temperature=25								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	77.17 °	> 45	83.94 °	81.36 °	1.08 °	11.2	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	28.03 m%	< 0.845	698.9 m%	251.1 m%	147.2 m%	1.34	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	439.6 m%	< 10	1.998 %	941.6 m%	334.7 m%	9.02	0
PH_ERR_MAX(3kHz)(summary)	100% (200/200)	69.39 m°	< 0.508	499.2 m°	198 m°	92.47 m°	1.12	0
DIFF_OFF(summary)	100% (200/200)	-5.813m	range -12.6m 12.6m	5.395m	24.1u	2.226m	1.88	0
I_ALL(summary)	100% (200/200)	103.6 uA	< 415	171.4 uA	143.8 uA	12.09 uA	1.14e+7	0
Yield Estimate: 98.5 %(197 passed/200 pts) | Parameters: vcm=2.25,VPOS=4.5,vd=2.65,temperature=170								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	80.73 °	> 45	85.84 °	83.61 °	922 m°	14	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	24.05 m%	< 0.845	698.1 m%	251.3 m%	148.1 m%	1.34	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	439.6 m%	< 10	2.391 %	979.2 m%	367.4 m%	8.18	0
PH_ERR_MAX(3kHz)(summary)	98.5% (197/200)	71.93 m°	< 0.508	594.5 m°	225.8 m°	103.9 m°	0.905	0
DIFF_OFF(summary)	100% (200/200)	-5.704m	range -12.6m 12.6m	5.33m	22.41u	2.182m	1.92	0
I_ALL(summary)	100% (200/200)	116.4 uA	< 415	168.1 uA	147.7 uA	9.378 uA	1.48e+7	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=2.25,VPOS=5,vd=2.65,temperature=-40								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	74.47 °	> 45	82.01 °	79.42 °	1.152 °	9.96	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	26.25 m%	< 0.845	764.1 m%	303.9 m%	161.3 m%	1.12	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	450.6 m%	< 10	1.96 %	932.1 m%	320.5 m%	9.43	0
PH_ERR_MAX(3kHz)(summary)	100% (200/200)	71.02 m°	< 0.508	469.6 m°	177.2 m°	83.64 m°	1.32	0
DIFF_OFF(summary)	100% (200/200)	-5.837m	range -12.6m 12.6m	5.406m	24.53u	2.235m	1.88	0
I_ALL(summary)	100% (200/200)	99.49 uA	< 415	181.1 uA	147.1 uA	14.42 uA	9.6e+6	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=2.25,VPOS=5,vd=2.65,temperature=25								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	76.46 °	> 45	82.72 °	80.32 °	1.01 °	11.7	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	30.67 m%	< 0.845	745.2 m%	290.7 m%	157.7 m%	1.17	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	439.2 m%	< 10	1.967 %	928.6 m%	323.1 m%	9.36	0
PH_ERR_MAX(3kHz)(summary)	100% (200/200)	64.99 m°	< 0.508	483.7 m°	186.5 m°	87.5 m°	1.22	0
DIFF_OFF(summary)	100% (200/200)	-5.802m	range -12.6m 12.6m	5.388m	23.94u	2.221m	1.89	0
I_ALL(summary)	100% (200/200)	107.2 uA	< 415	175.2 uA	147.5 uA	12.15 uA	1.14e+7	0
Yield Estimate: 99 %(198 passed/200 pts) | Parameters: vcm=2.25,VPOS=5,vd=2.65,temperature=170								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	79.91 °	> 45	84.82 °	82.59 °	886.1 m°	14.1	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	29.33 m%	< 0.845	732.4 m%	278.9 m%	155.1 m%	1.22	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	441.5 m%	< 10	2.133 %	957.6 m%	341.2 m%	8.83	0
PH_ERR_MAX(3kHz)(summary)	99% (198/200)	69.69 m°	< 0.508	547.3 m°	212.5 m°	96.94 m°	1.02	0
DIFF_OFF(summary)	100% (200/200)	-5.699m	range -12.6m 12.6m	5.327m	22.37u	2.18m	1.92	0
I_ALL(summary)	100% (200/200)	119.2 uA	< 415	171 uA	150.6 uA	9.413 uA	1.47e+7	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=2.25,VPOS=5.5,vd=2.65,temperature=-40								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	74.33 °	> 45	81.36 °	78.95 °	1.093 °	10.4	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	29.43 m%	< 0.845	820.2 m%	345.6 m%	170.5 m%	0.976	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	487.7 m%	< 10	1.945 %	933.4 m%	309.4 m%	9.77	0
PH_ERR_MAX(3kHz)(summary)	100% (200/200)	70.93 m°	< 0.508	461 m°	171.5 m°	79.61 m°	1.41	0
DIFF_OFF(summary)	100% (200/200)	-5.829m	range -12.6m 12.6m	5.401m	24.4u	2.232m	1.88	0
I_ALL(summary)	100% (200/200)	103.2 uA	< 415	185 uA	150.8 uA	14.47 uA	9.56e+6	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: vcm=2.25,VPOS=5.5,vd=2.65,temperature=25								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	76.13 °	> 45	81.98 °	79.74 °	956.7 m°	12.1	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	31.13 m%	< 0.845	795.6 m%	325.8 m%	167.3 m%	1.03	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	469.4 m%	< 10	1.95 %	929.8 m%	313.5 m%	9.64	0
PH_ERR_MAX(3kHz)(summary)	100% (200/200)	72.42 m°	< 0.508	474.7 m°	180.4 m°	83.62 m°	1.31	0
DIFF_OFF(summary)	100% (200/200)	-5.795m	range -12.6m 12.6m	5.384m	23.85u	2.219m	1.89	0
I_ALL(summary)	100% (200/200)	110.8 uA	< 415	179.2 uA	150.9 uA	12.19 uA	1.13e+7	0
Yield Estimate: 99 %(198 passed/200 pts) | Parameters: vcm=2.25,VPOS=5.5,vd=2.65,temperature=170								
CS_IP_Equalizers_Diff_Mill_swc_1								
PhaseMargin_Diff(summary)	100% (200/200)	79.41 °	> 45	84.07 °	81.93 °	841.7 m°	14.6	0
MAX_ERR_NORM(3kHz)(summary)	100% (200/200)	29.79 m%	< 0.845	774.9 m%	309.6 m%	163.5 m%	1.09	0
MAX_ERR_NORM(20kHz)(summary)	100% (200/200)	460.7 m%	< 10	2.069 %	949.7 m%	327.8 m%	9.2	0
PH_ERR_MAX(3kHz)(summary)	99% (198/200)	71.04 m°	< 0.508	522.4 m°	203.3 m°	92.51 m°	1.1	0
DIFF_OFF(summary)	100% (200/200)	-5.697m	range -12.6m 12.6m	5.325m	22.36u	2.179m	1.92	0
I_ALL(summary)	100% (200/200)	126.9 uA	< 415	180.5 uA	156.3 uA	9.495 uA	1.46e+7	0

Figure A.2: Complete results of Monte Carlo simulations 5 V device